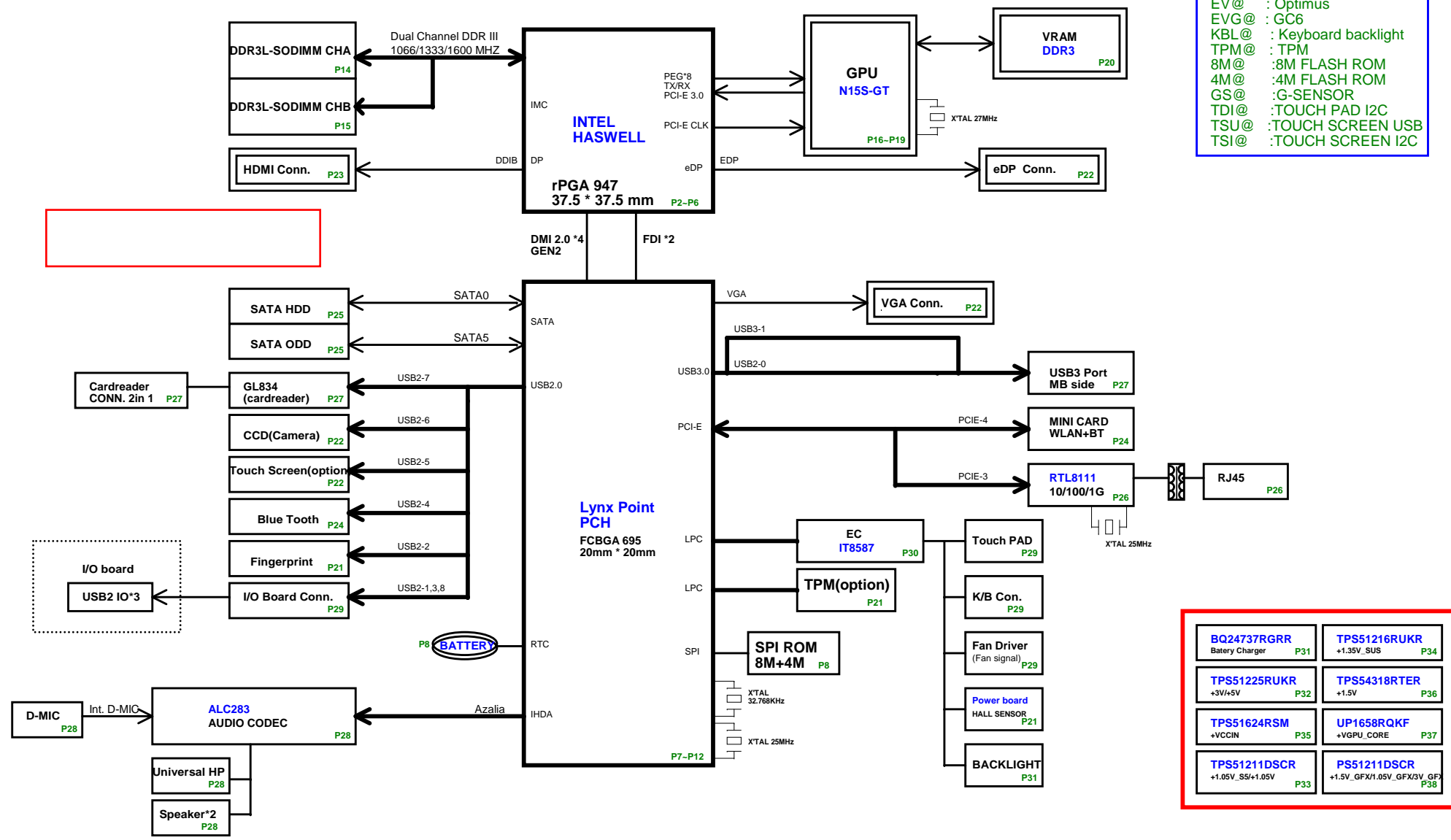


Z8B_GDDR3 HSW SV SYSTEM BLOCK DIAGRAM

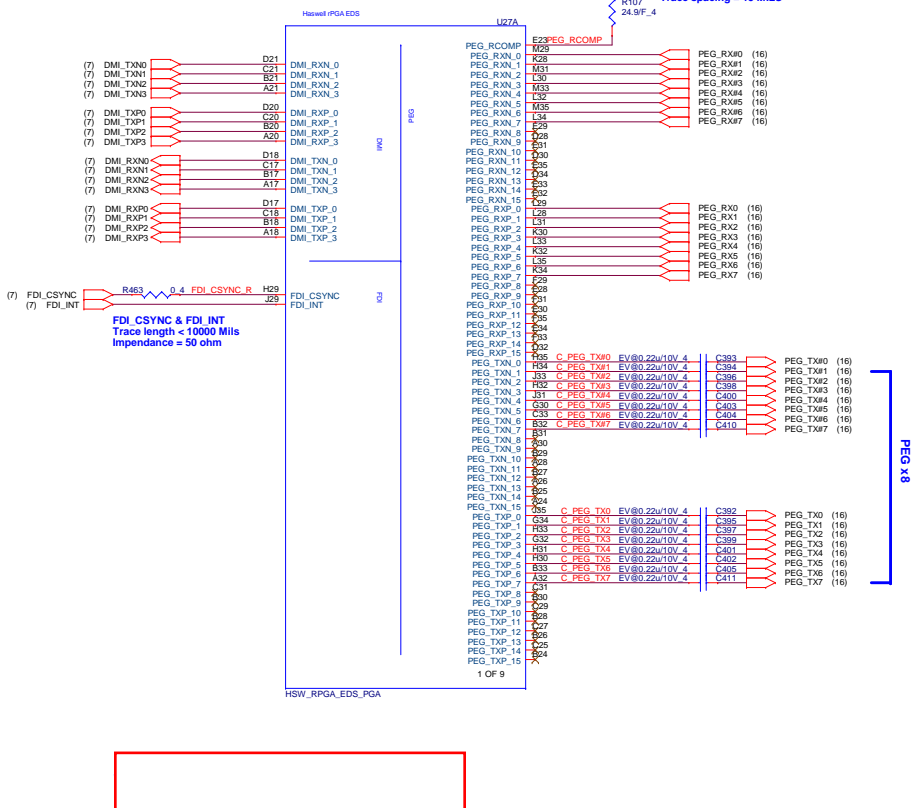
BOM

- IV@ : iGPU
- EV@ : Optimus
- EVG@ : GC6
- KBL@ : Keyboard backlight
- TPM@ : TPM
- 8M@ : 8M FLASH ROM
- 4M@ : 4M FLASH ROM
- GS@ : G-SENSOR
- TDI@ : TOUCH PAD I2C
- TSU@ : TOUCH SCREEN USB
- TSI@ : TOUCH SCREEN I2C

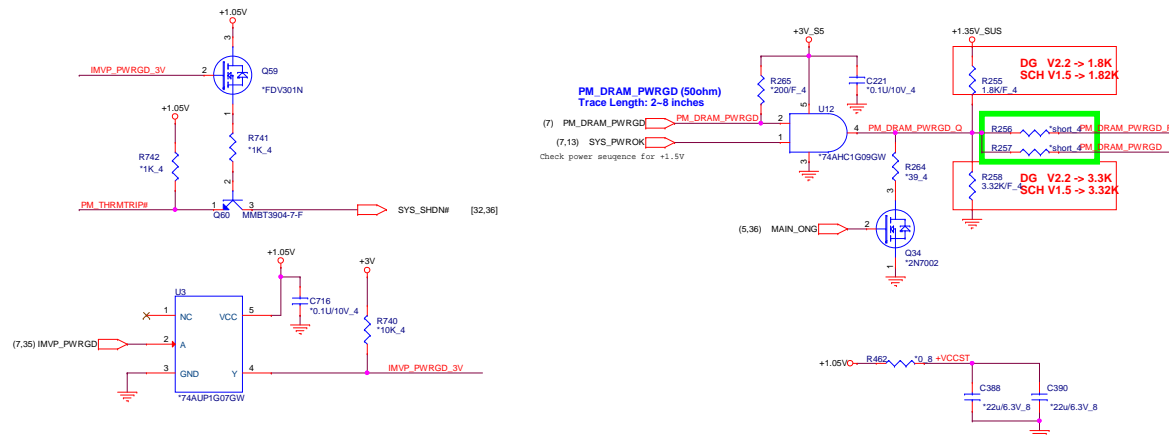
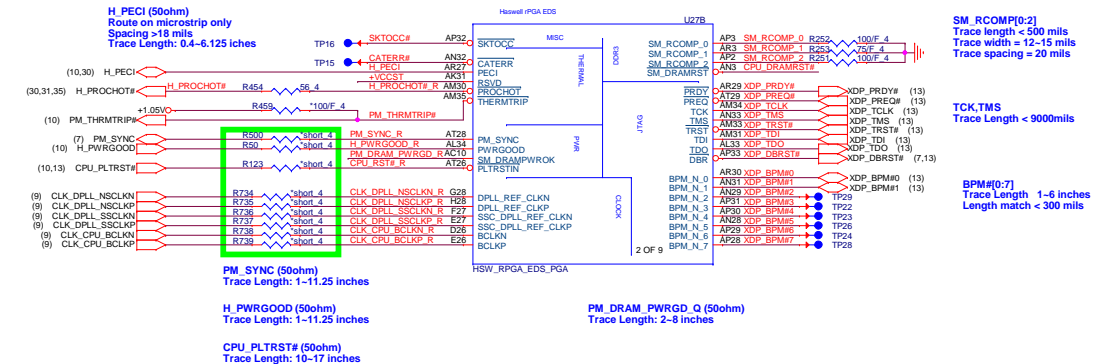


BQ24737RGRR Battery Charger P31	TPS51216RUKR +1.35V_SUS P34
TPS51225RUKR +3V/+5V P32	TPS54318RTER +1.5V P36
TPS51624RSM +VCCIN P35	UP1658RQKF +VGPU_CORE P37
TPS51211DSCR +1.05V_SS/+1.05V P33	PS51211DSCR +1.5V_GFX/1.05V_GFX/3V_GFX P38

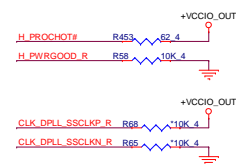
Haswell Processor (DMI,PEG,FDI)



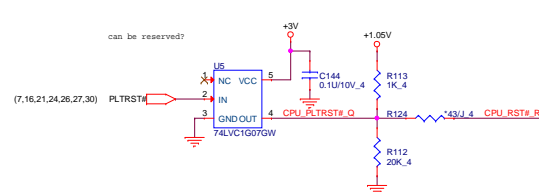
Haswell Processor (CLK,MISC,JTAG)



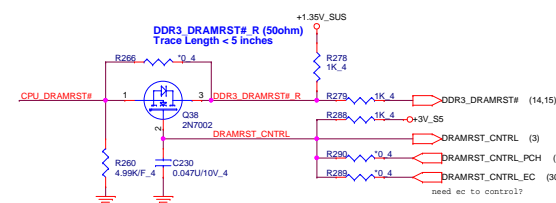
PU/PD of CPU



Reserved For buffer reset of PLTRSRIN#



SM_DRAMRST# Topology



XDP PU/PD

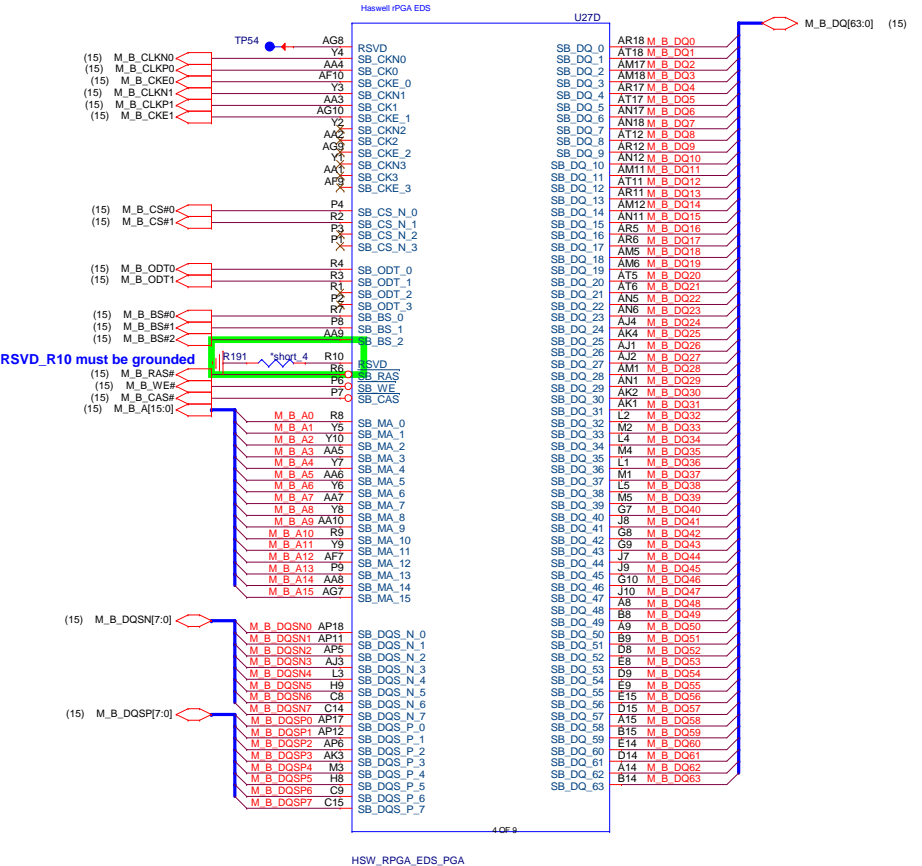
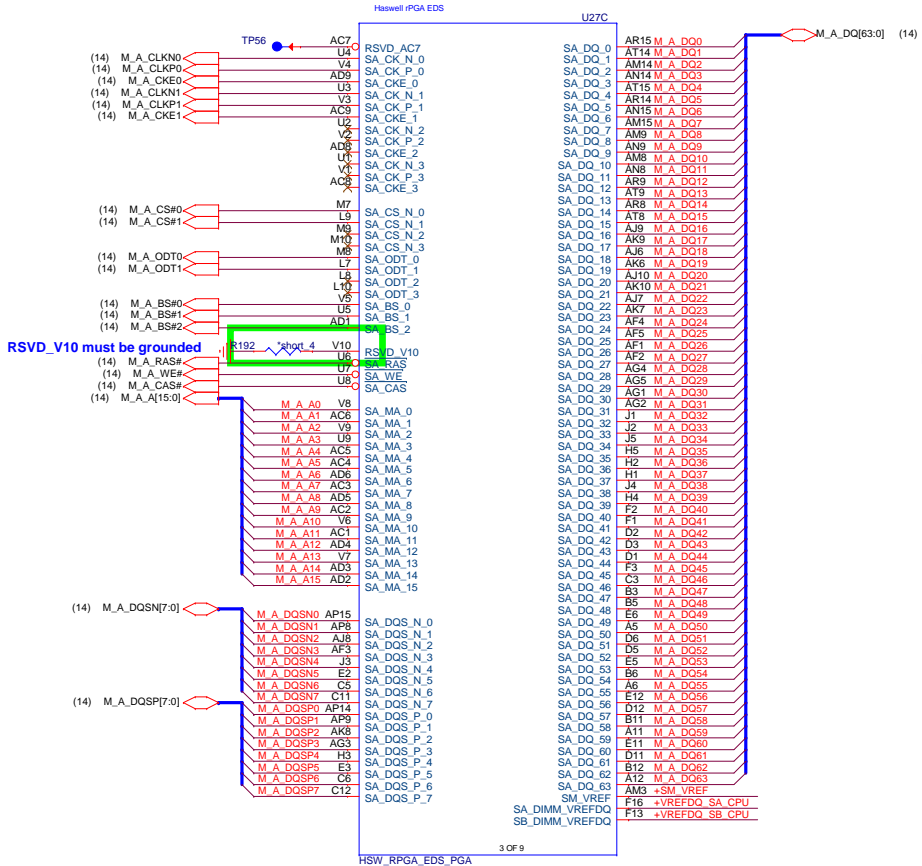


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PROJECT : Z8B

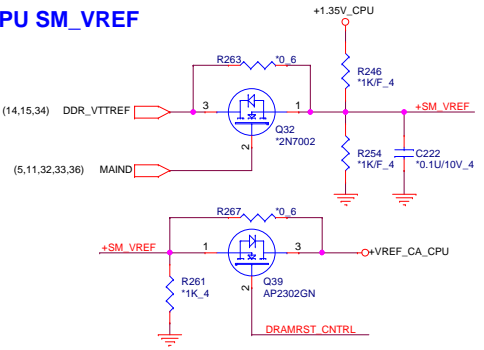
Size	Document Number	R
	Haswell 1/5 (PEG/DWI/FDI)	
Date:	Monday, July 14, 2014	Sheet 2 of 44

Haswell Processor (DDR3)

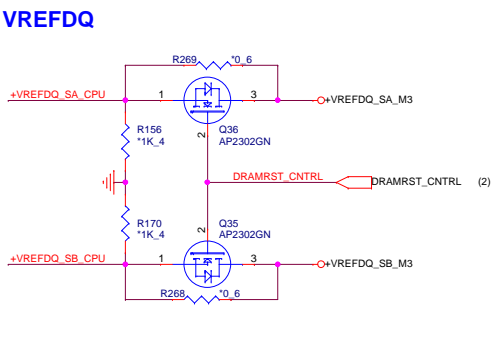
Haswell Processor (DDR3)



CPU SM_VREF

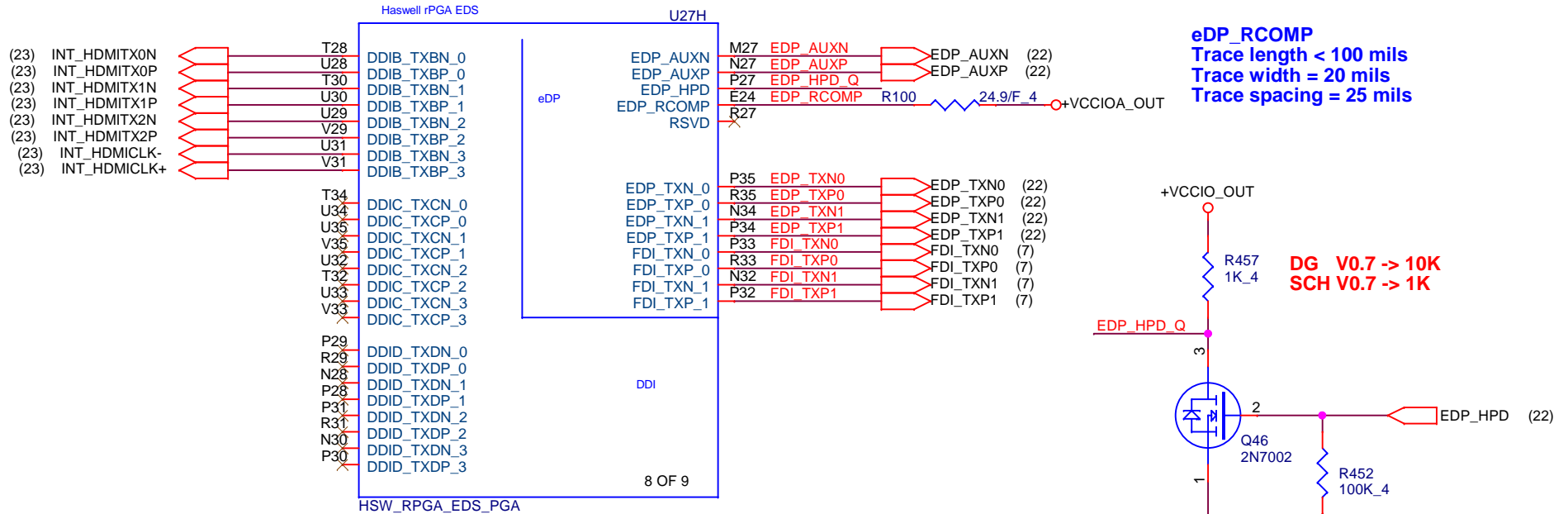


CPU VREFDQ



Haswell Processor (DDI,eDP,FDI)

HDMI



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PROJECT : Z8B

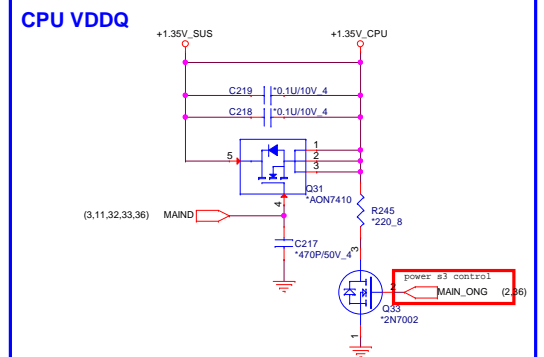
Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	1A

Date: Friday, June 13, 2014 Sheet 4 of 44

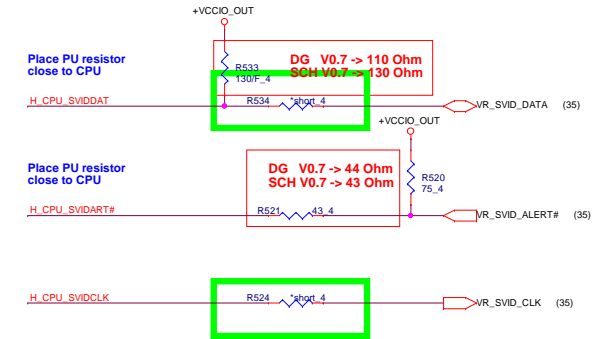
Haswell rPGA EDS



470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity



Layout note: need routing together and ALERT need between CLK and DATA.



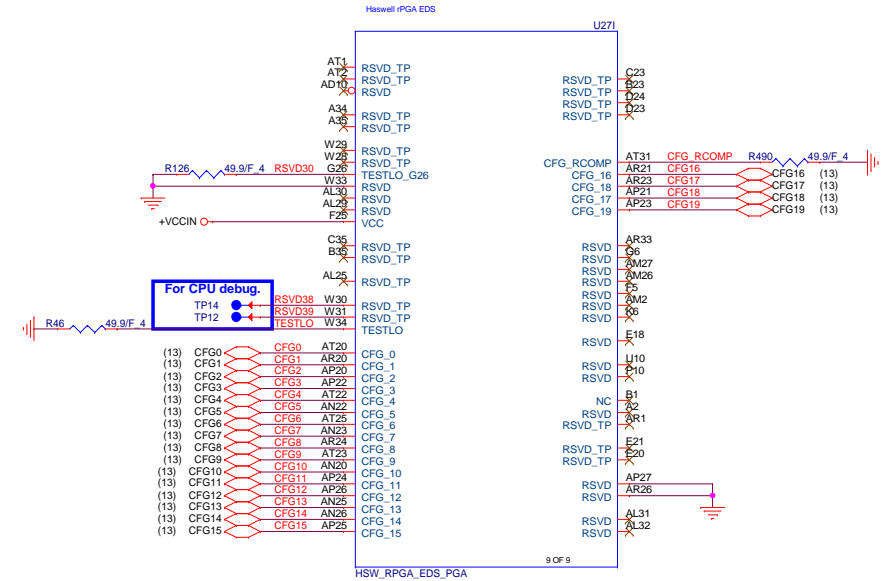
PROJECT : Z8B

Size	Document Number Haswell 4/5 (POWER)	Rev 1A
Date:	Monday, July 14, 2014	Sheet 5 of 44

Haswell Processor (GND)

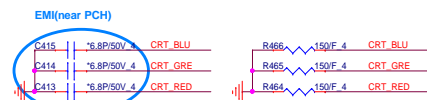
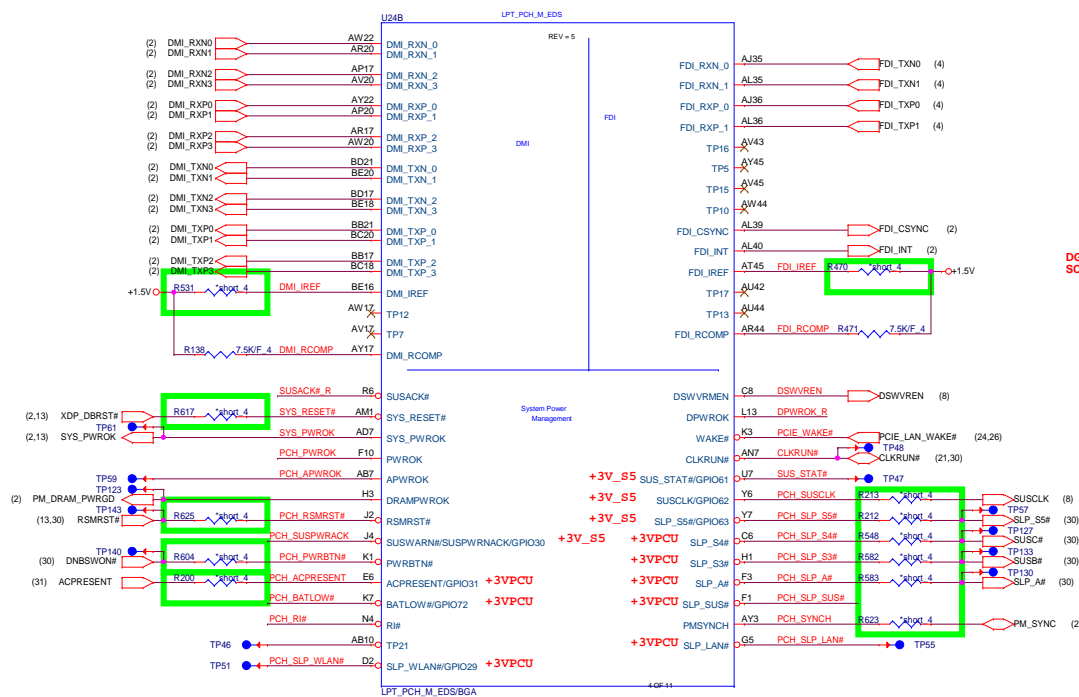


Haswell Processor (CFG,RSVD)

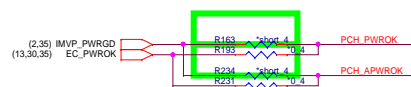
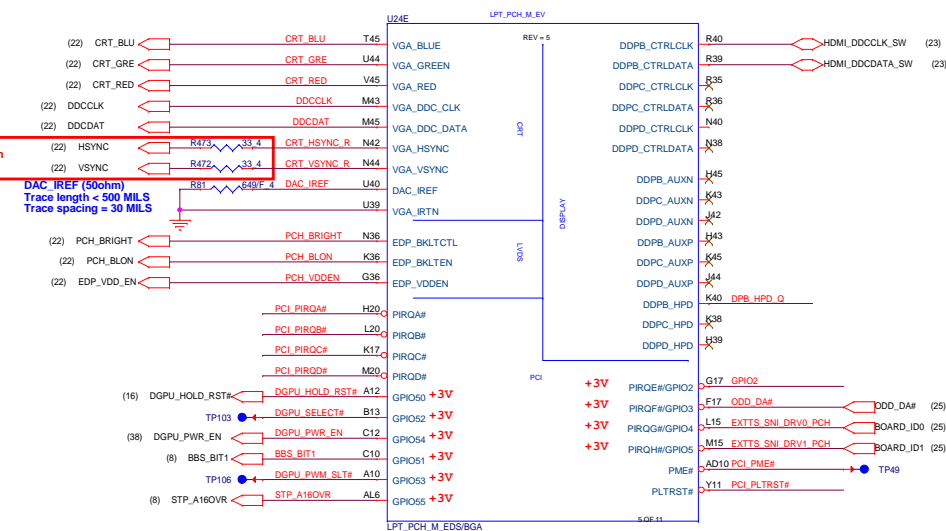


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	

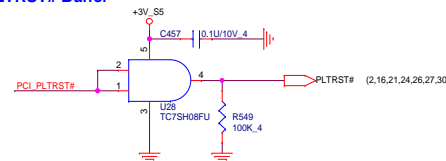
Lynx Point (DMI,FDI,PM)



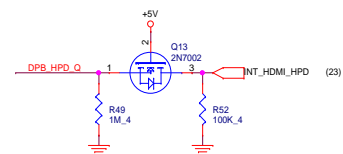
Lynx Point (CRT,PCI,DDI CNTL)



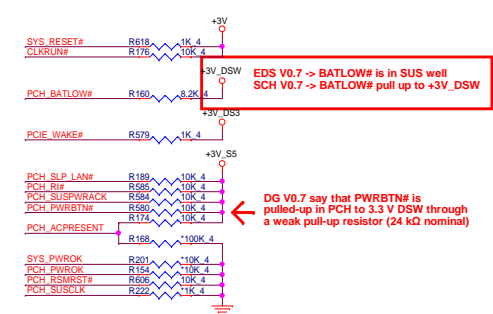
PLTRST# Buffer



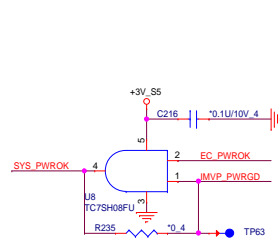
HDMI HPD



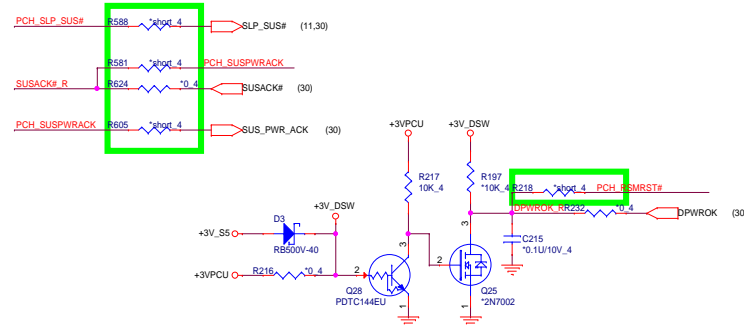
PCH PM PU/PD



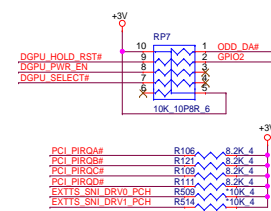
SYSPWOK



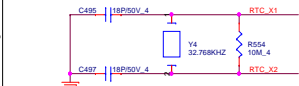
DSW Circuit



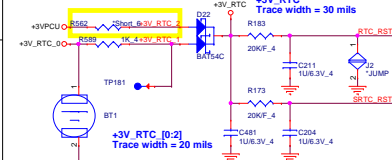
PCI PU



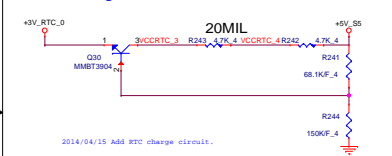
RTC Clock 32.768KHz (RTC)



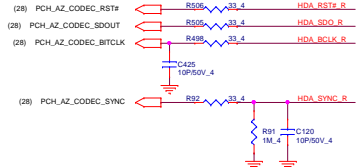
RTC Circuitry (RTC)



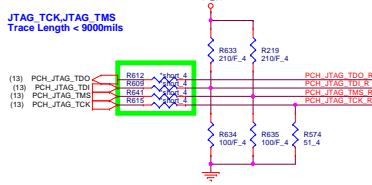
RTC charge circuit



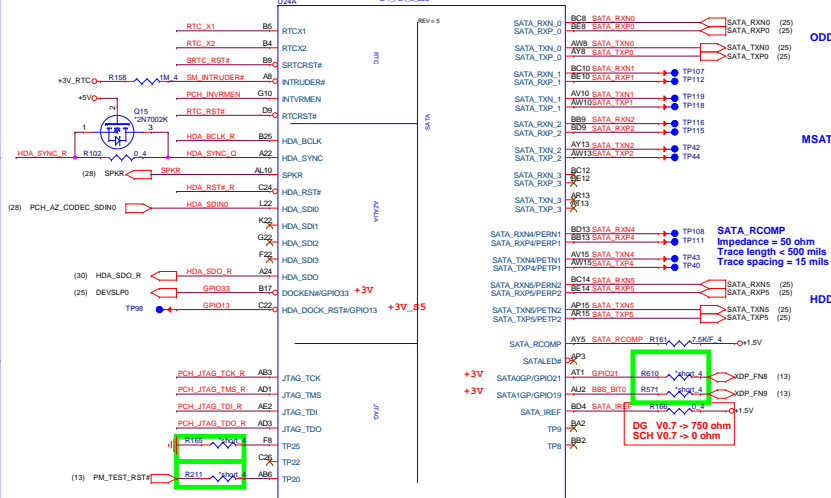
HDA



PCH JTAG



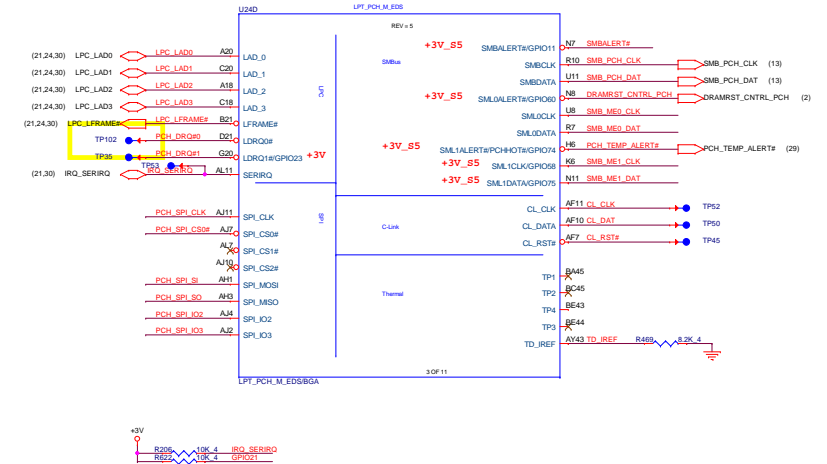
Lynx Point (RTC, I2C, SATA, JTAG)



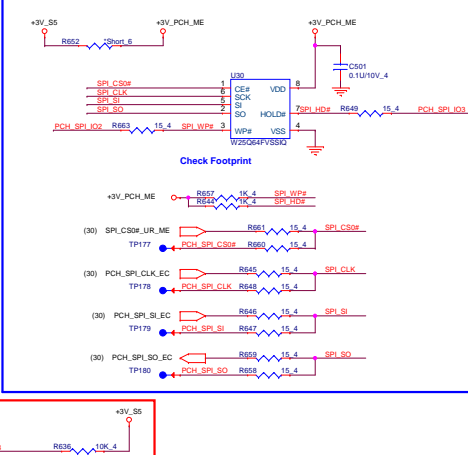
PCH STRAPPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	SPKR R209 10K 4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(7) SUSCLK R221 10K 4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(7) STP_A180VR R167 10K 4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R171 390K 4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Reversed 0 0 LFC	(7) BBS_BT0 R146 10K 4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	(7) BBS_BT0 R146 10K 4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	HDA_SDO_R R501 10K 4 +VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	(10) GPIO36 R696 10K 4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(10) FDL0VR/LT0 R620 10K 4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	(10,22) GPIO8 R601 10K 4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(10) PLL_OVR_EN R155 10K 4
DSWREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(7) DSWREN R164 330K 4 +3V_RTC

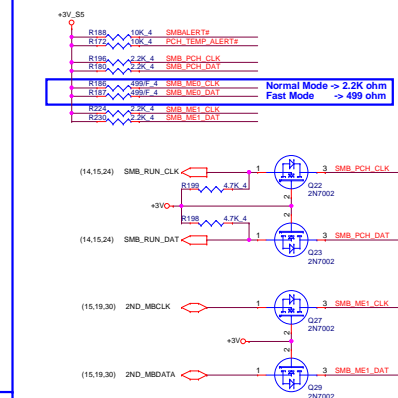
Lynx Point (LPC, SPI, SMBUS, C-LINK, THERMAL)



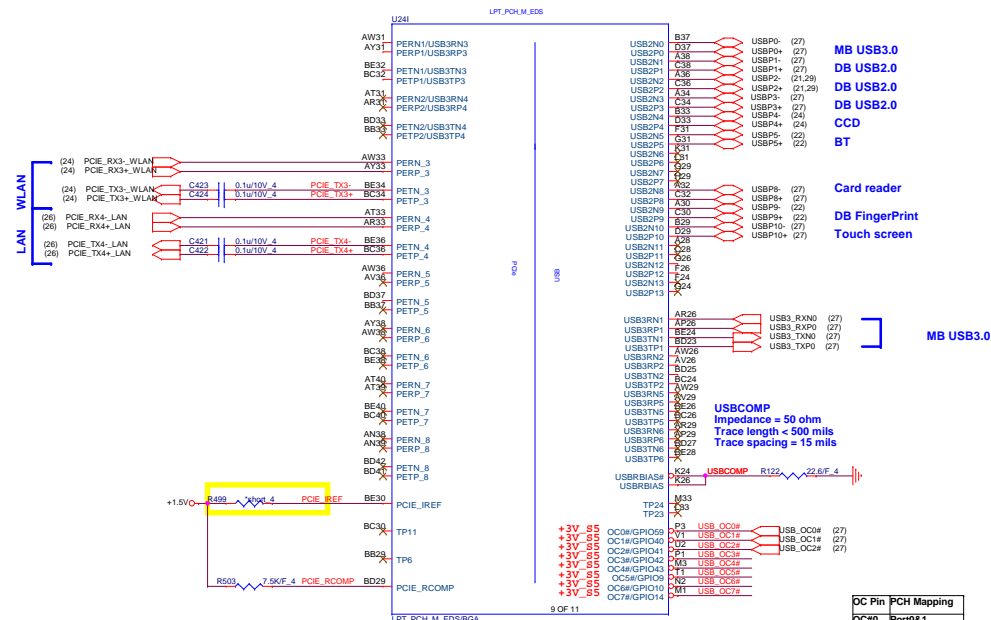
PCH Quad SPI ROM



SMBus

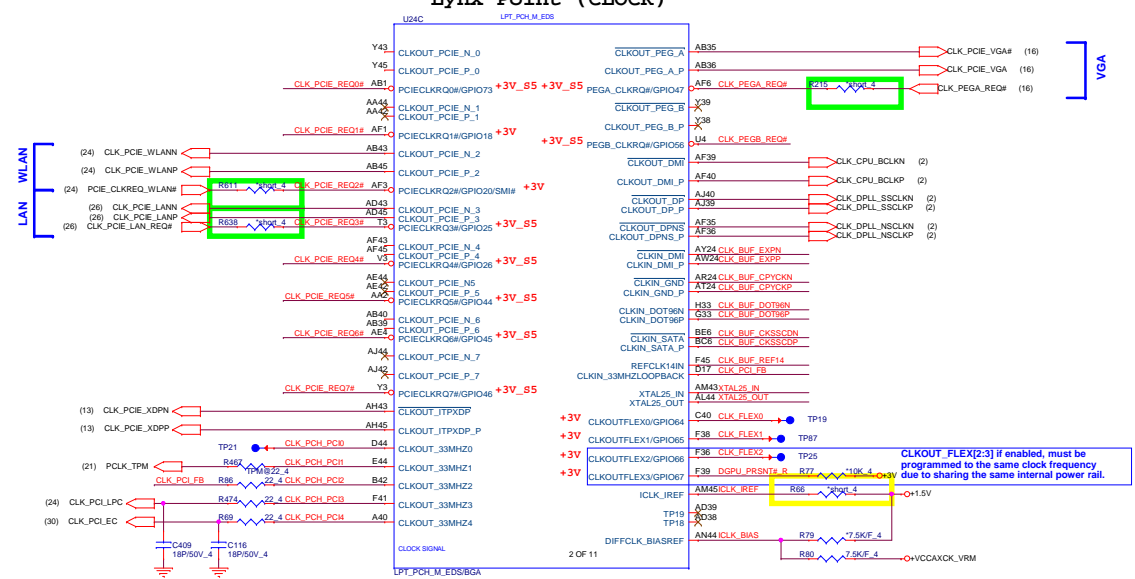


Lynx Point (PCIe,USB3.0,USB2.0)

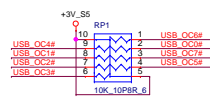


OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

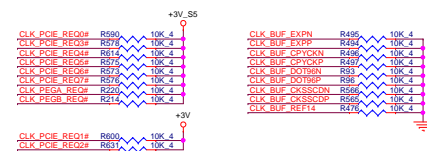
Lynx Point (CLOCK)



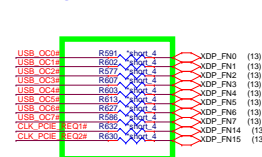
USB Overcurrent



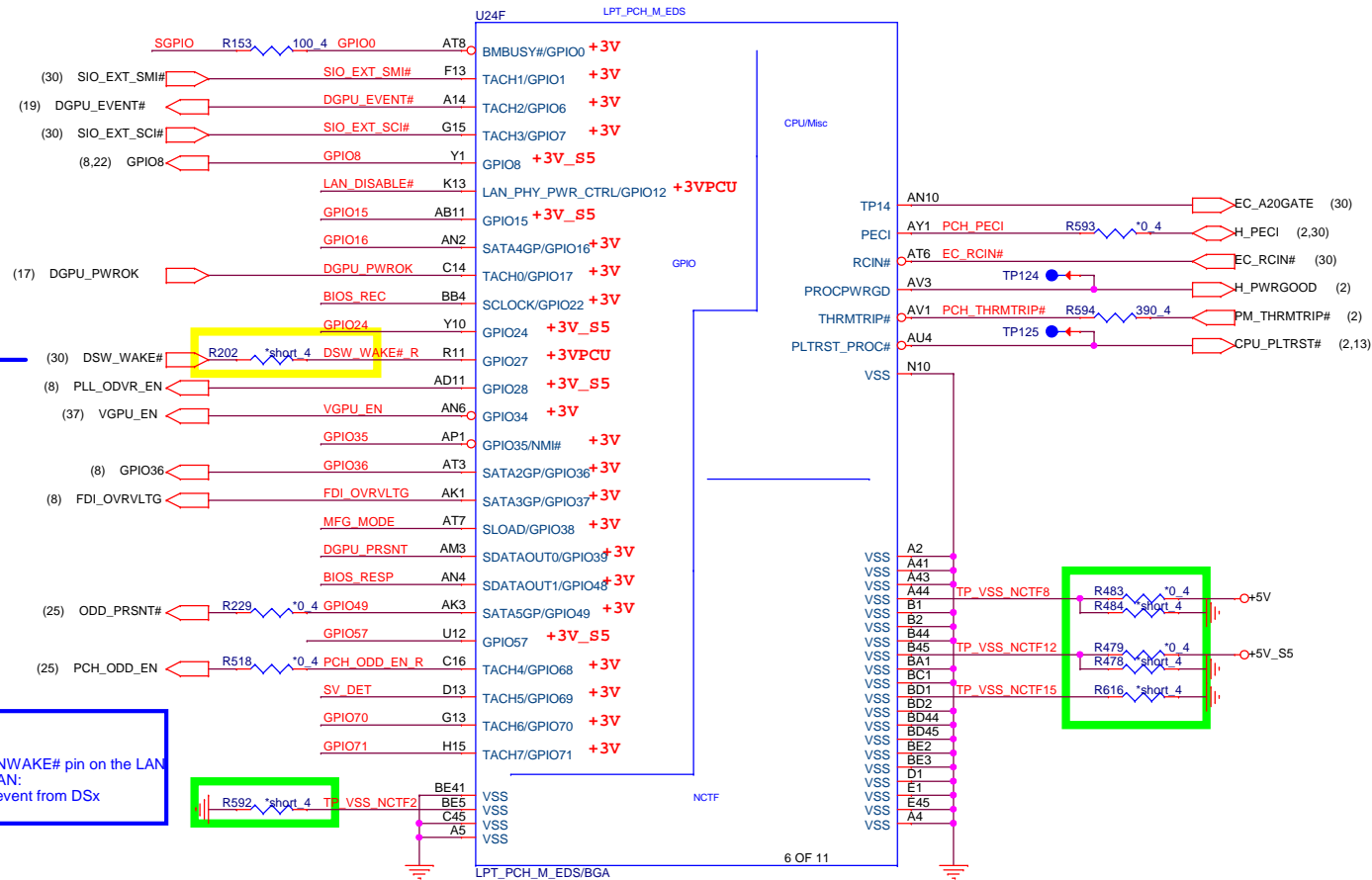
PCH Internal Clock



PCH XDP Signal Routed by 50 ohm



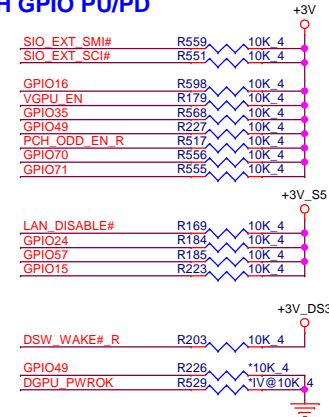
Lynx Point (GPIO,CPU/MISC,NCTF)



XDP Signal

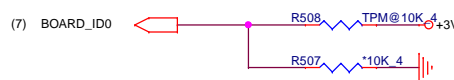


PCH GPIO PU/PD



BOARD ID

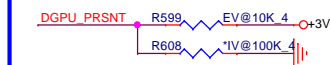
TPM exist or not
0 = No TPM
1 = TPM exist



Reserve:
0 = No xxx
1 = xxx exist

External Gfx Present

0 = Internal Gfx
1 = External Gfx



PCH MISC PU/PD



BIOS RECOVERY

0 = Enable
1 = Disable



Swap GPIO

0 = SGPIO
1 = Default



MFG TEST



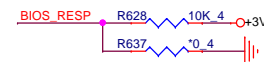
SV Detect

0 = SV Detect
1 = Default



BIOS_RESP

0 = BIOS RESP
1 = Default

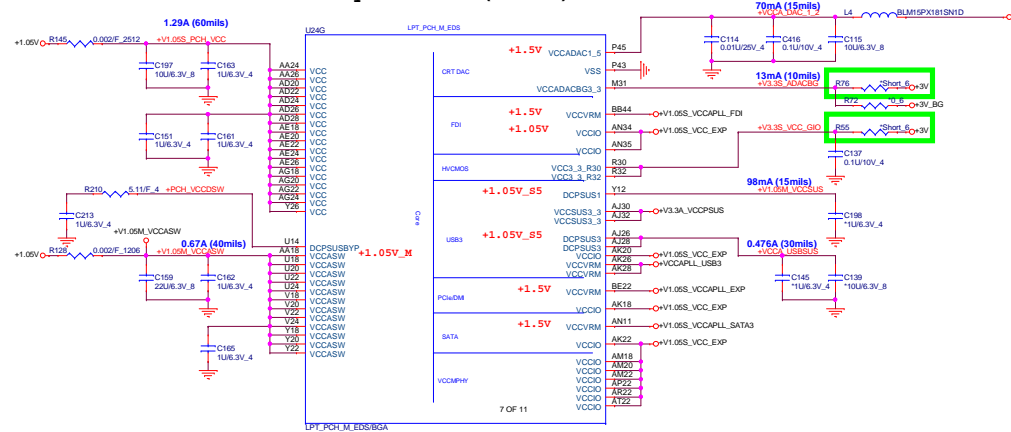


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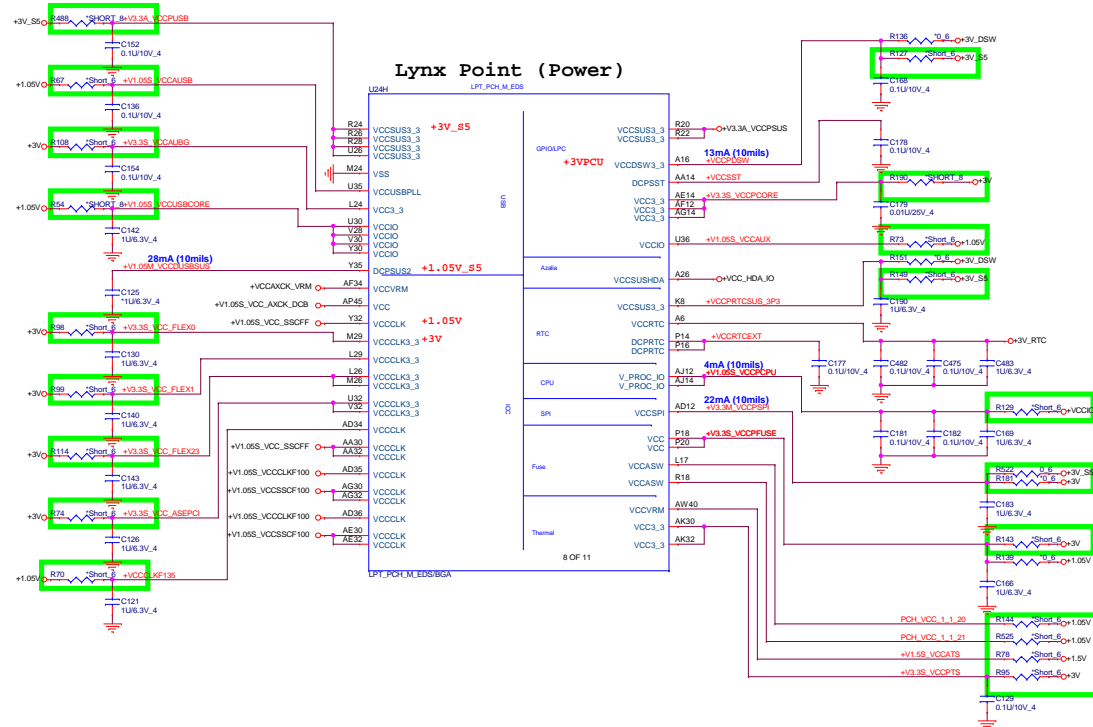
PROJECT : Z8B

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
Date:	Wednesday, July 09, 2014	Sheet 10 of 44

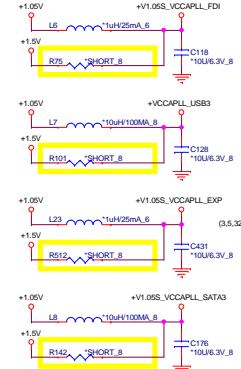
Lynx Point (Power)



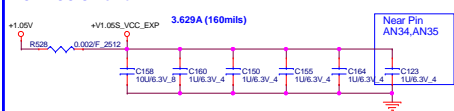
Lynx Point (Power)



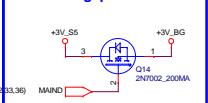
PCH VRM Power 1.05V OPTION IS PROVIDED
0.179A (20mils) FOR VALIDATION PURPOSES



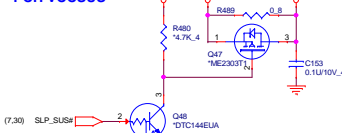
3 PCH VCCIO Power



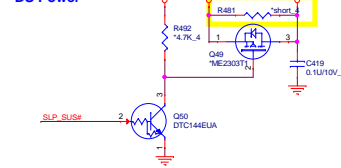
PCH band gap Power



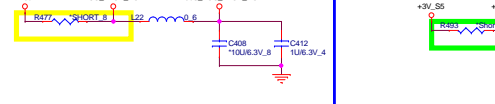
PCH VCCSUS



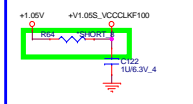
DS Power

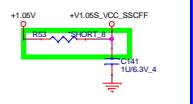
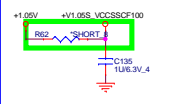


PCH HDA Power	0.0
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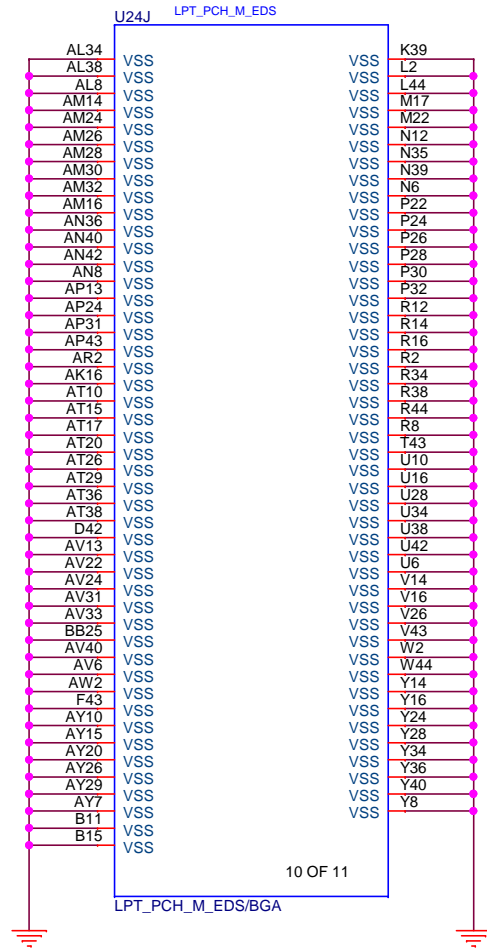


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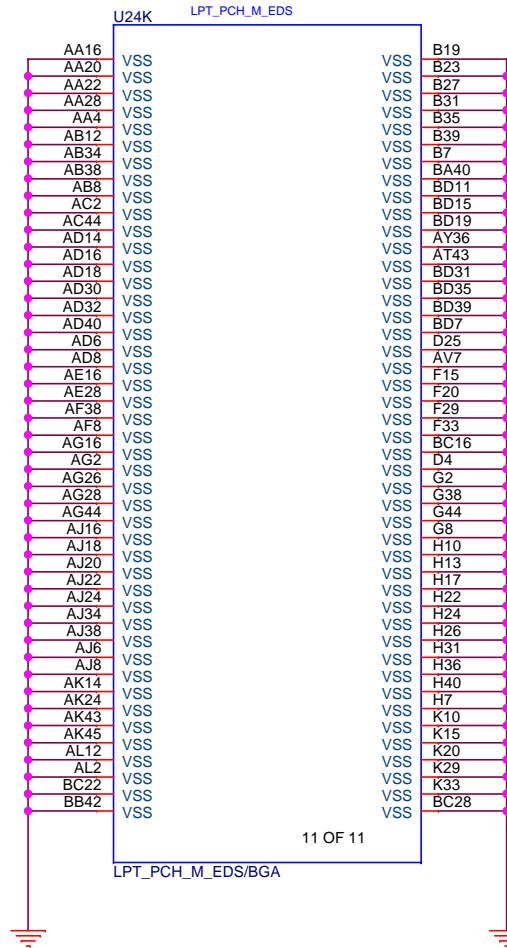


[illegible]

Lynx Point (GND)



Lynx Point (GND)



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PROJECT : Z8B

Size	Document Number	Rev
	LPT 6/6 (GND)	1A
Date:	Tuesday, May 13, 2014	Sheet 12 of 44

(9) CLK_PCIE_XDPP R744 *short 4 CLK_PCIE_XDPP_R
(9) CLK_PCIE_XDPN R745 *short 4 CLK_PCIE_XDPN_R

+1.05V R71 51 4 XDP_TDO

(6) CFG0 R567 *short 4 OBSDAT_A0
(6) CFG1 R563 *short 4 OBSDAT_A1
(6) CFG2 R152 *short 4 OBSDAT_A2
(6) CFG3 R561 *short 4 OBSDAT_A3
(6) CFG4 R148 *short 4 OBSDAT_B0
(6) CFG5 R141 *short 4 OBSDAT_B1
(6) CFG6 R110 *short 4 OBSDAT_B2
(6) CFG7 R132 *short 4 OBSDAT_B3
(21,30) NBSWON# R532 *short 4 CPU_HOOK1
R274 *short 4 PCH_HOOK1
(5) PWR_DEBUG R87 *short 4 CPU_HOOK2
(2,7) XDP_DBRST# R486 *short 4 CPU_HOOK7
R485 *short 4 PCH_HOOK7

(8) SMB_PCH_CLK Q55 2N7002 1 R678 4.7K 4
Q54 2N7002 1 R677 4.7K 4
(8) SMB_PCH_DAT Q54 2N7002 1 R677 4.7K 4

+3V_S5
R642 210/F_4
PCH_JTAG_TDO
R640 100/F_4

CPU XDP

(2) XDP_PREQ# XDP_PREQ# TP94
(2) XDP_PRDY# XDP_PRDY# TP93
OBSDAT_A0 TP120
OBSDAT_A1 TP126
OBSDAT_A2 TP41
OBSDAT_A3 TP121
OBSDAT_B0 TP39
OBSDAT_B1 TP37
OBSDAT_B2 TP31
OBSDAT_B3 TP34
CPU_HOOK1 TP104
CPU_HOOK2 TP162
CLK_PCIE_XDPP_R TP85
CLK_PCIE_XDPN_R TP86
CPU_HOOK7 TP91
SMB_XDP_DAT TP97
SMB_XDP_CLK TP162
(2) XDP_TDO XDP_TDO TP20
(2) XDP_TRST# XDP_TRST# TP18
(2) XDP_TDI XDP_TDI TP90
(2) XDP_TMS XDP_TMS TP88
(2) XDP_TCLK XDP_TCLK TP17
TP64
TP11
TP62

TP84
TP83
TP95
TP92
TP110
TP113
TP100
TP114
TP129
TP105
TP122
TP117
TP99
TP30
TP96
TP97
TP68
TP13
TP109
TP155
TP157
TP176
OBSFN_B0
OBSFN_B1
OBSFN_C0
OBSFN_C1
OBSFN_C2
OBSFN_C3
OBSFN_D0
OBSFN_D1
OBSDAT_D0
OBSDAT_D1
OBSDAT_D2
OBSDAT_D3
CPU_HOOK0
CPU_HOOK6

0.4A (20mils)
+VCC_CPU_XDP +VCCIO_OUT
C407 *0.1U/10V_4
C391 *0.1U/10V_4
R458 *short 4

Stuff R1016, R1138
No stuff R1017, R1137

OBSFN_B0 R491 *short 4 XDP_BPM#0 (2)
OBSFN_B1 R487 *short 4 XDP_BPM#1 (2)
OBSFN_C0 R545 *short 4 CFG17 (6)
R544 *0.4 CFG16 (6)
OBSFN_C1 R547 *0.4 CFG17
R546 *short 4 CFG16
OBSDAT_C0 R516 *short 4 CFG8 (6)
OBSDAT_C1 R550 *short 4 CFG9 (6)
OBSDAT_C2 R587 *short 4 CFG10 (6)
OBSDAT_C3 R539 *short 4 CFG11 (6)
OBSFN_D0 R557 *short 4 CFG19 (6)
R558 *0.4 CFG18 (6)
OBSFN_D1 R552 *0.4 CFG19
R553 *short 4 CFG18
OBSDAT_D0 R504 *short 4 CFG12 (6)
OBSDAT_D1 R103 *short 4 CFG13 (6)
OBSDAT_D2 R502 *short 4 CFG14 (6)
OBSDAT_D3 R511 *short 4 CFG15 (6)
CPU_HOOK0 R51 1K 4 H_PWRGOOD_R (2)
CPU_HOOK6 R540 1K 4 CPU_PLTRST# (2,10)
CPU_HOOK3 R277 *short 4 SPS_PWROK (2,7)

PCH XDP

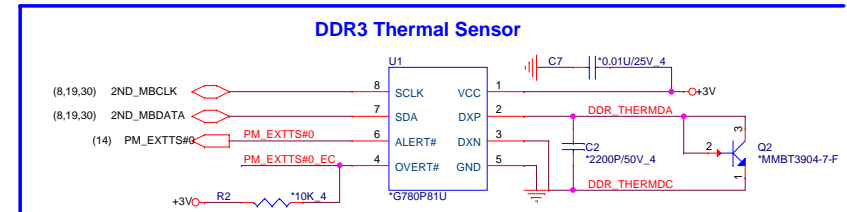
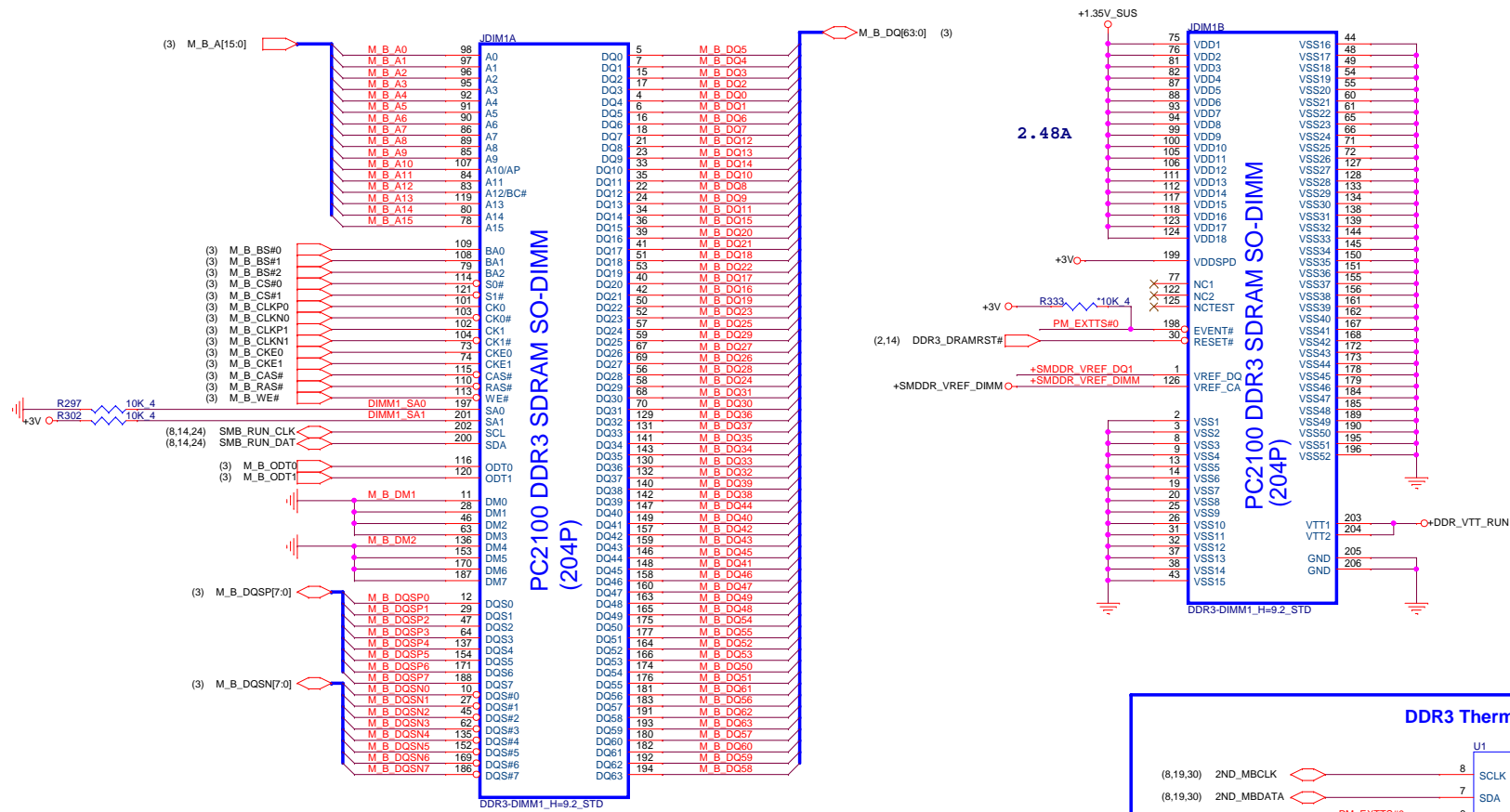
(9) XDP_FN0 XDP_FN0 TP142
(9) XDP_FN1 XDP_FN1 TP138
(9) XDP_FN2 XDP_FN2 TP134
(9) XDP_FN3 XDP_FN3 TP148
(9) XDP_FN4 XDP_FN4 TP152
(9) XDP_FN5 XDP_FN5 TP145
(9) XDP_FN6 XDP_FN6 TP147
(9) XDP_FN7 XDP_FN7 TP131
PCH_HOOK1 TP66
+1.05V TP101
PCH_HOOK7 TP89
SMB_XDP_DAT TP158
SMB_XDP_CLK TP161
PCH_JTAG_TDO TP144
PM_TEST_RST# TP58
(8) PCH_JTAG_TDI PCH_JTAG_TDI TP137
(8) PCH_JTAG_TMS PCH_JTAG_TMS TP154
(8) PCH_JTAG_TCK PCH_JTAG_TCK TP149
TP164
TP77
TP159

+VCC_PCH_XDP +3V_S5
R720 *short 4
TP168
TP167
TP141
TP128
TP139
TP132
TP136
TP146
XDP_FN_CLK1
XDP_FN_CLK2
XDP_FN8
XDP_FN9
XDP_FN10
XDP_FN11
XDP_FN12
XDP_FN13
XDP_FN14
XDP_FN15
TP135
TP60
TP151
TP150
TP153
TP72
TP71
TP76
TP74
R639 1K 4
R326 1K 4
RSMRST# (7,30)
EC_PWROK (7,30,35)

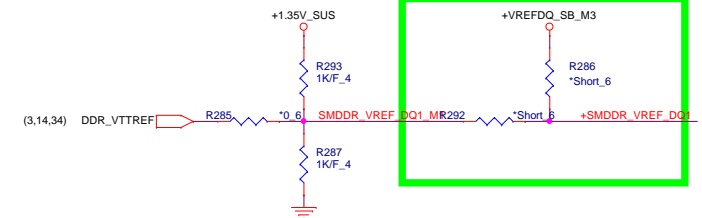


Quanta Computer Inc.
PROJECT : Z8B

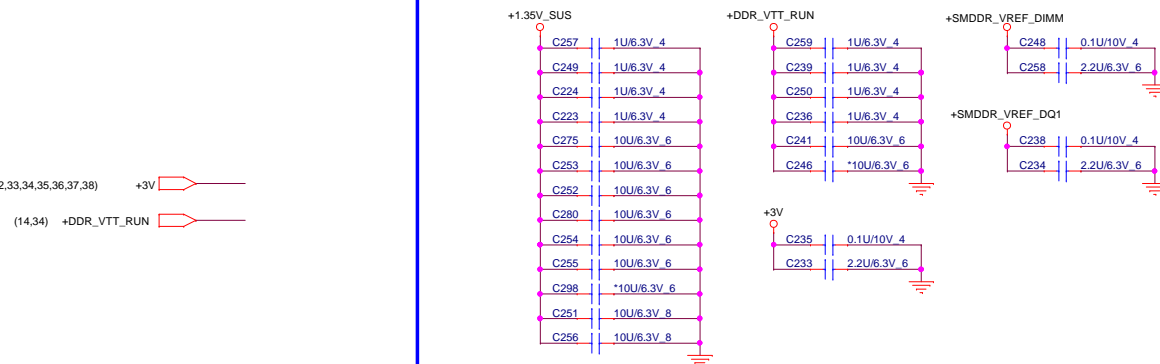
[illegible]

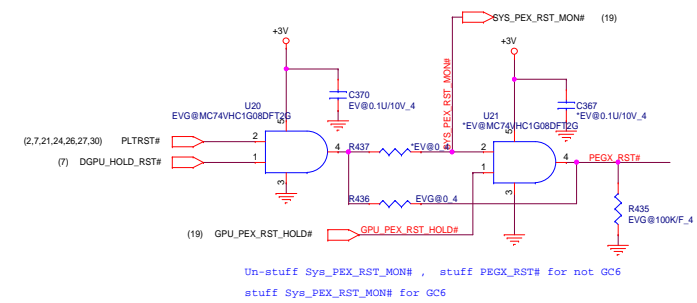
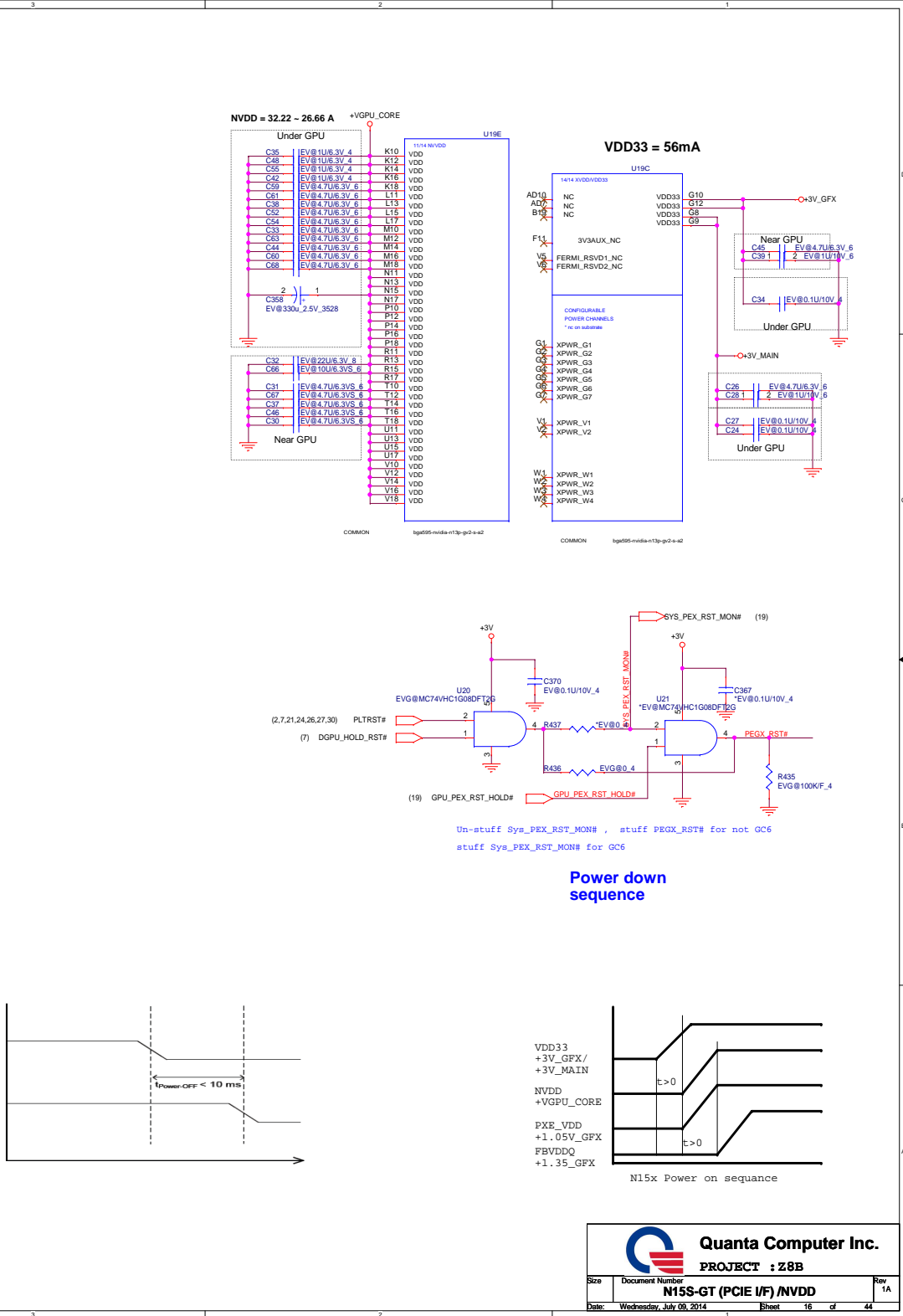


VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.





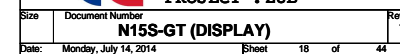
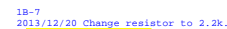
VDD33
+3V_GFX/
+3V_MAIN

NVDD
+VGPU_CORE

FXE_VDD
+1.05V_GFX

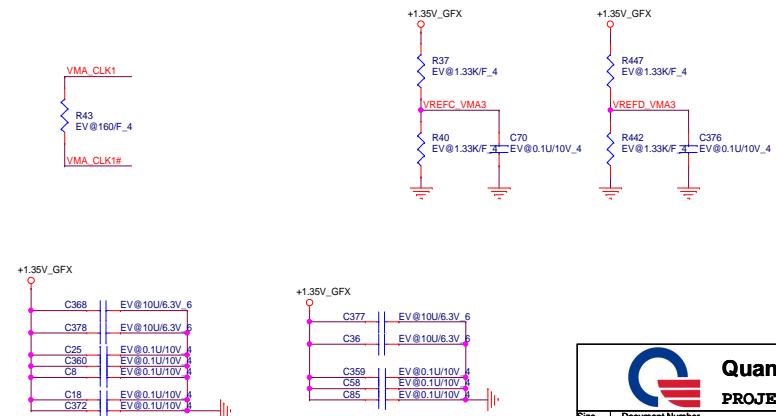
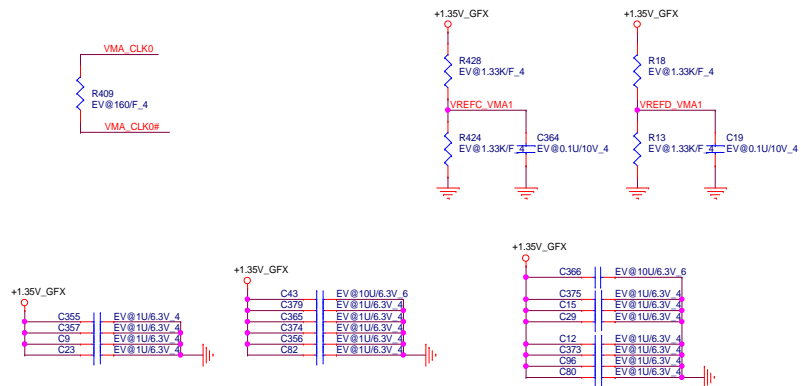
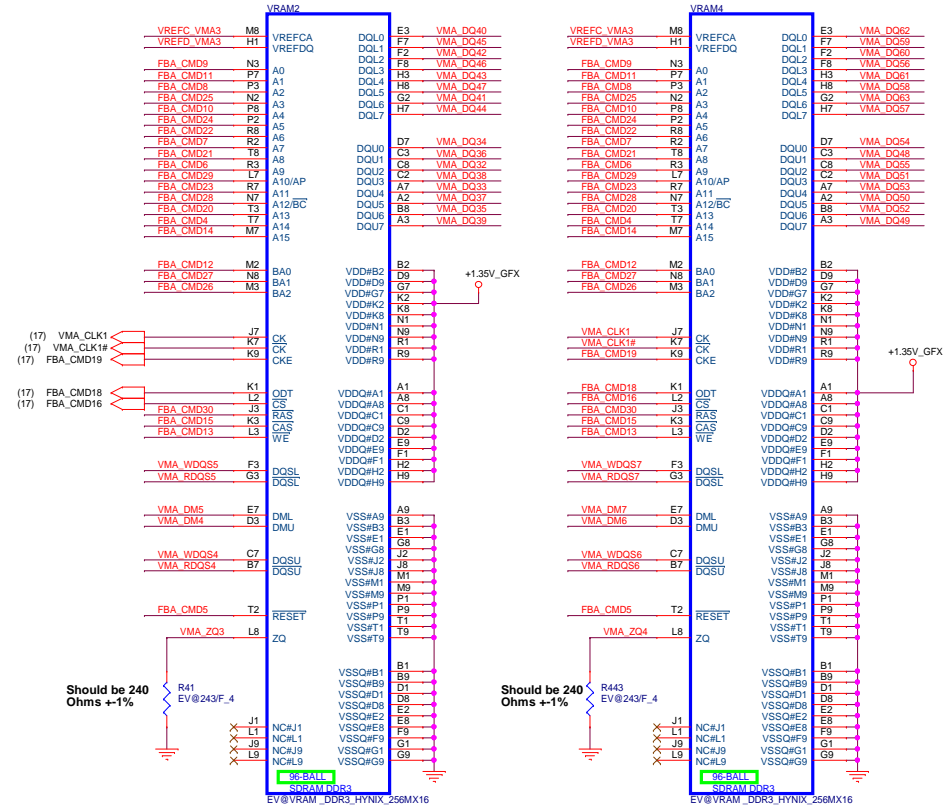
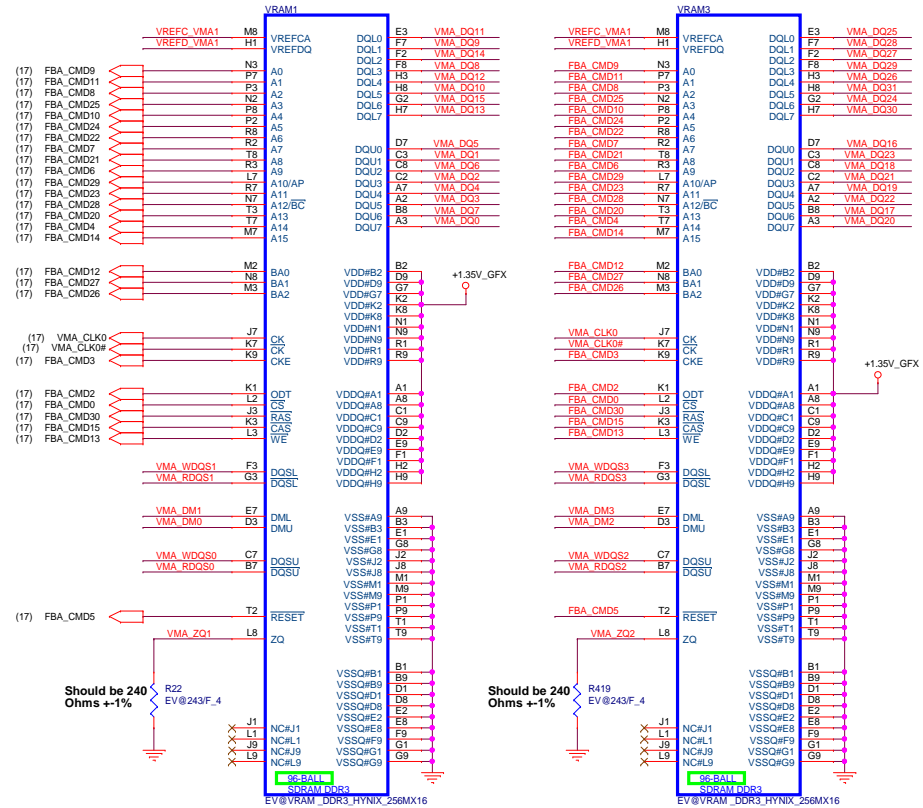
FBVDDQ
+1.35_GFX

N15x Power on sequence



CHANNEL A: 256MB/512MB DDR3

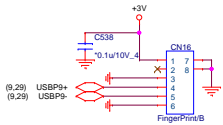
HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
QBC TOP B/S
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534



DP TO VGA

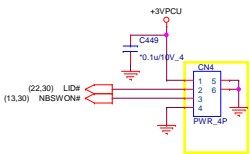
1A-1 2013/10/15 Change VGA ITE soltion to NXP.
1A-5 2013/10/18 Change VGA NXP soltion to ITE.

FingerPrint Conn



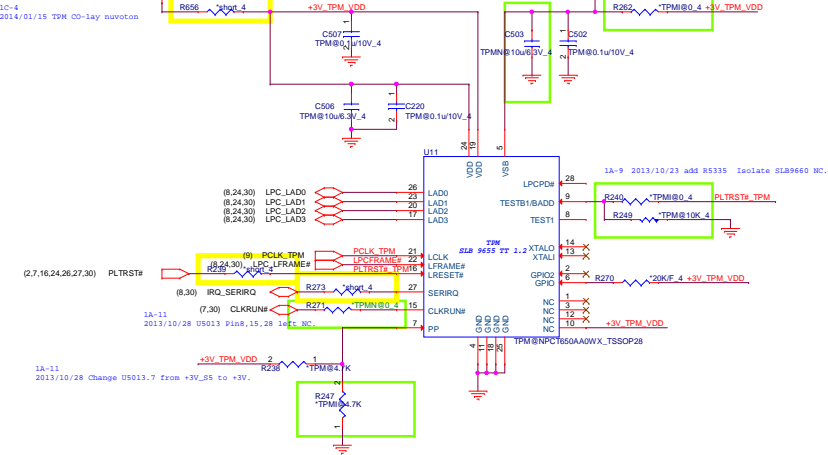
1A-7 2013/10/22 Change CN4 to 6pin.
1B-6 2013/12/18 Change CN5 USB port to port2.

Power Button/Conn



1A-1 2013/10/15 change to 6pin.
1B-2 2013/12/3 change to 4pin.
1B-3 2013/12/10 change CN6 footprint.

TPM



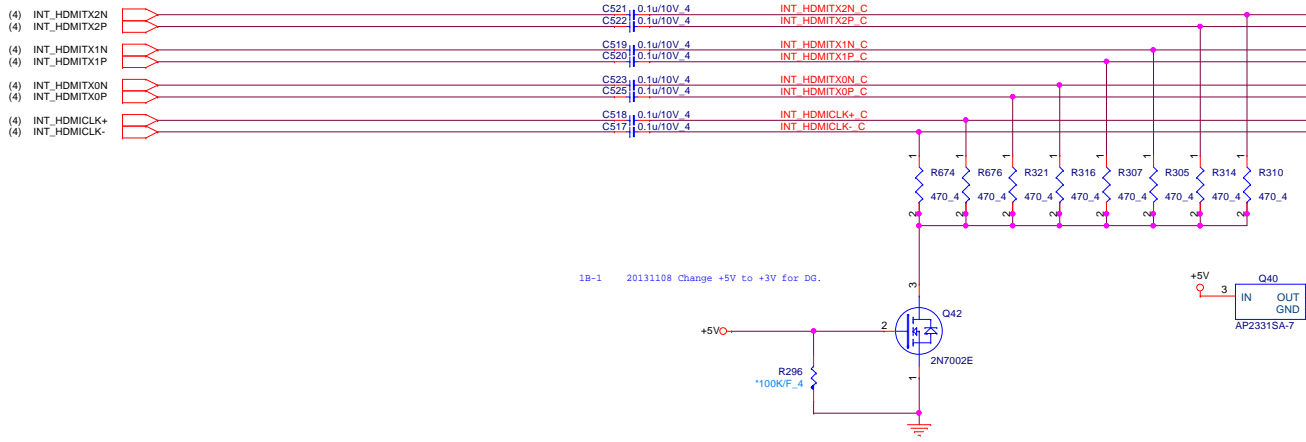
TPM1@-->for SLB9655		
TPM0@-->for NuvoTon		
R259	Un-stuff	stuff
C503	Un-stuff	stuff
R271	Un-stuff	stuff
R247	stuff	Un-stuff
R240	stuff	Un-stuff
R262	stuff	Un-stuff

Green CLK Gen

1B-4 2013/12/13 remove Green CLK U9

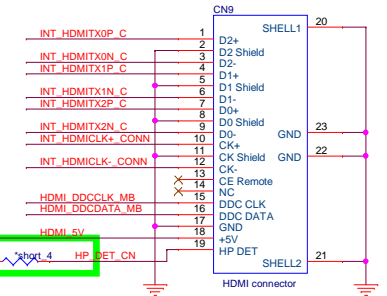
HDMI

From PCH

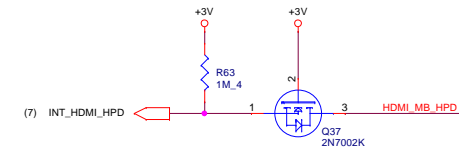


INT_HDMICLK+ C R301 *shot_4 INT_HDMICLK+ CONN
INT_HDMICLK- C R299 *shot_4 INT_HDMICLK- CONN

HDMI connector



HDMI-detect

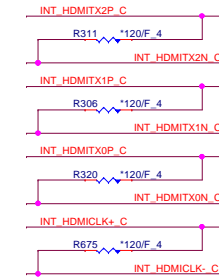


I2C

From PCH



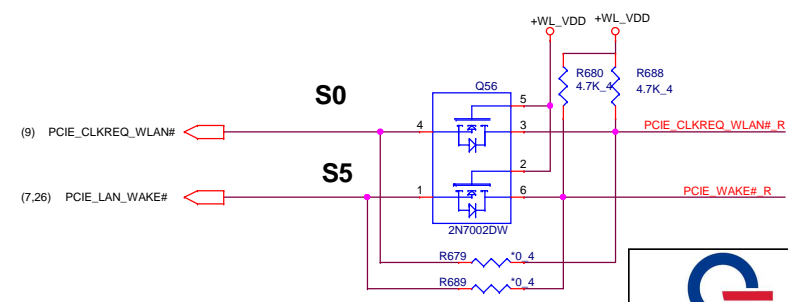
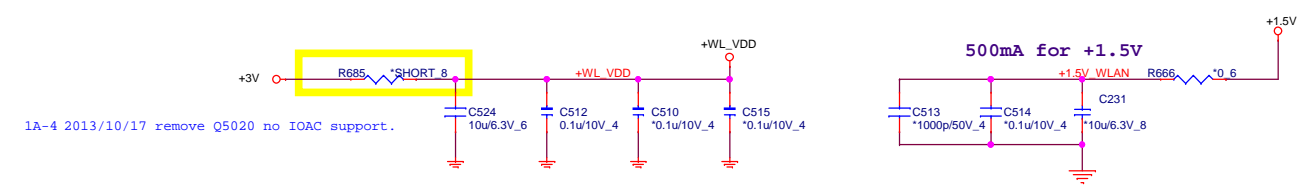
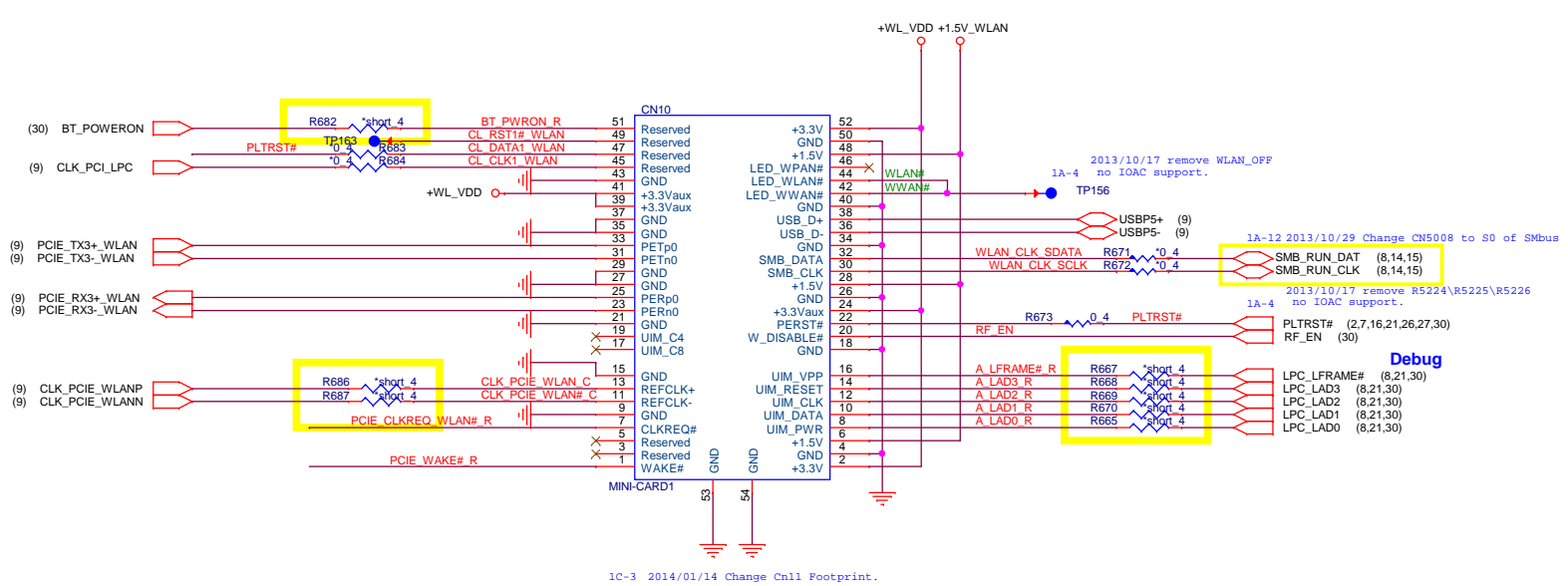
EMI



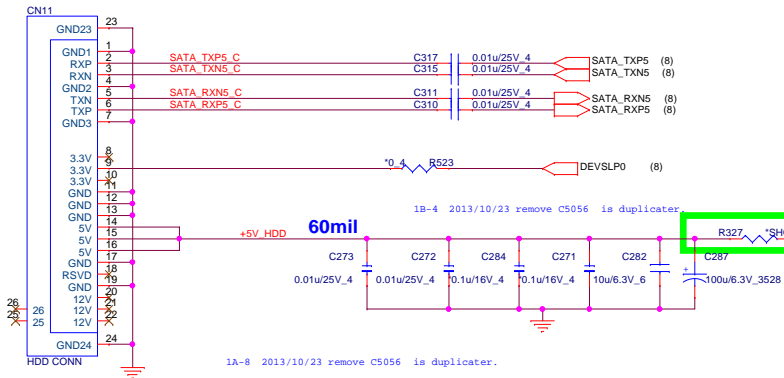
Power trace tracking

(2,7,8,9,10,11,13,14,15,16,17,18,21,22,24,25,26,27,28,29,30,32,33,34,35,36,37,38) +3V
(7,8,10,21,22,25,28,29,32,36) +5V

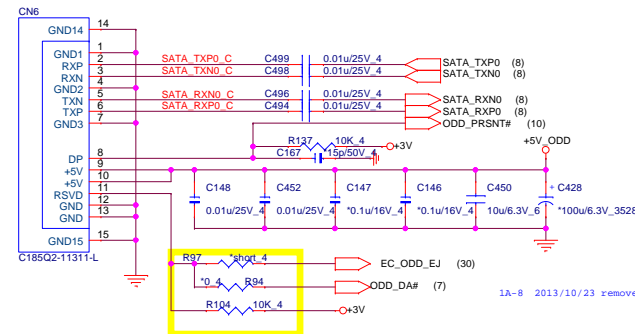
24 Mini Card 1 (MNC)



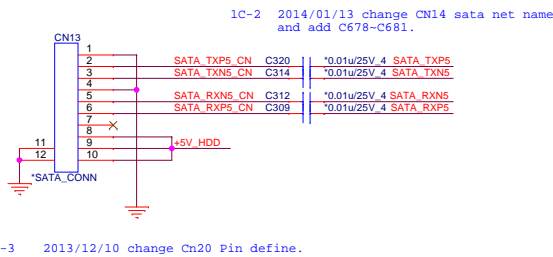
25 2.5" SATA HDD (HDD)



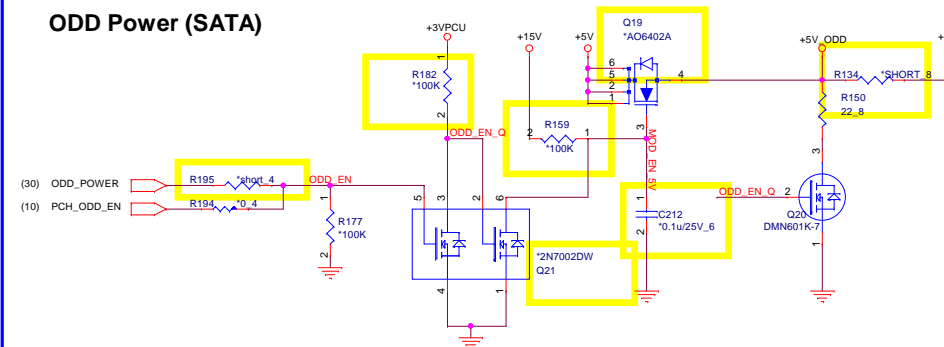
SATA ODD Connector



FFC Type SATA HDD CON

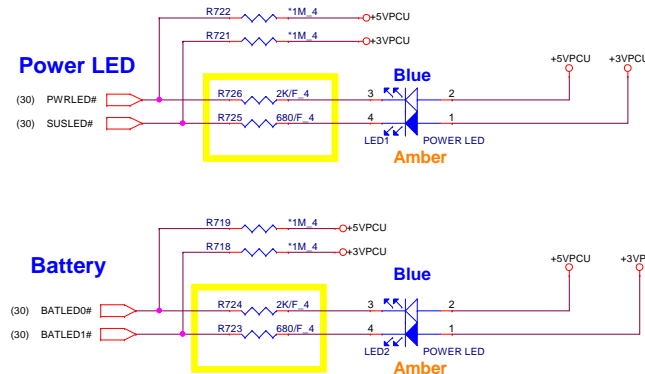


ODD Power (SATA)



POWER LED

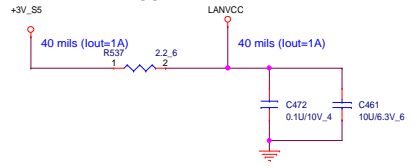
- 1A-9 2013/10/17 Change power LED from +3VPCU to +3V_S5.
- 1A-10 2013/10/25 change LED from 3pin to 4pin.
- 1A-11 2013/10/28 change LED from 4pin to 3pin.
- 1B-2 2013/12/03 change LED from 3pin to 4pin.
- 1C1-1 2014/02/06 change Blue LED power rail to +5VPCU.



Power trace tracking



LANVCC



For RTL8111GS
* Place 0.1uF CAP close to each
VDD33 pin-- 11, 32

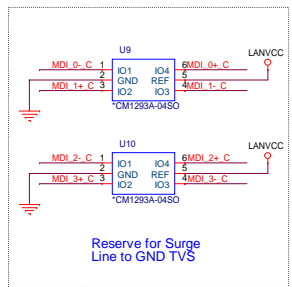
For Surge improvement
C5117/C5111 close
to pin 11,23.

Remove For Not Using SWR mode
C824,C825 close to Pin23.

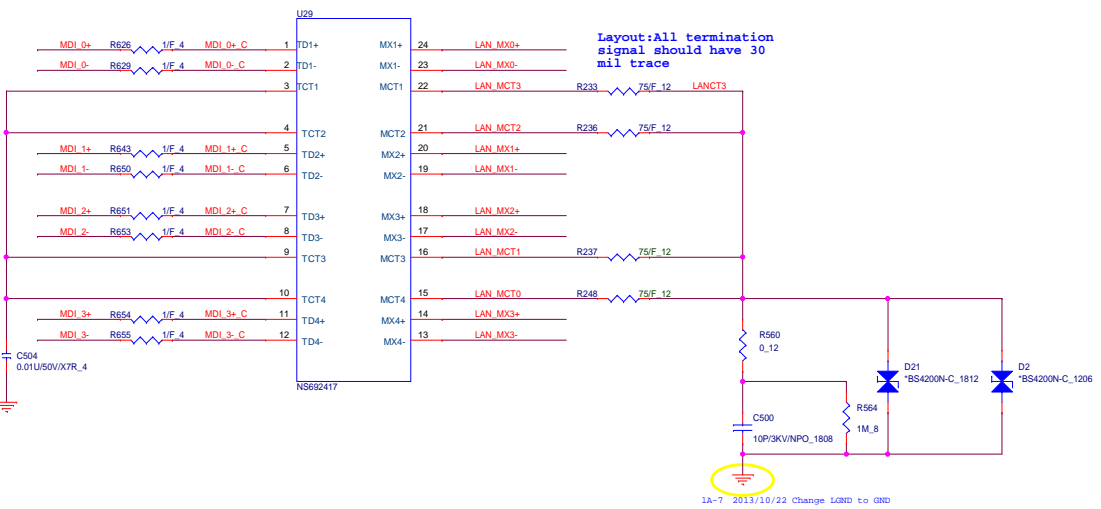
For RTL8111G(S)
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

For RTL8111G(S)
* Place 0.1uF CAP close to each
VDD10 pin-- 3, 8, 22, 30

Transformer

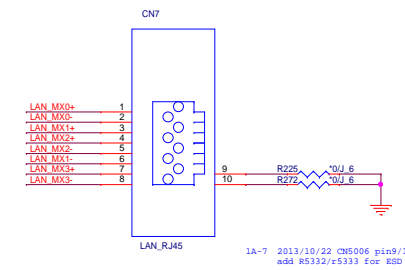


Reserve for Surge
Line to GND TVS



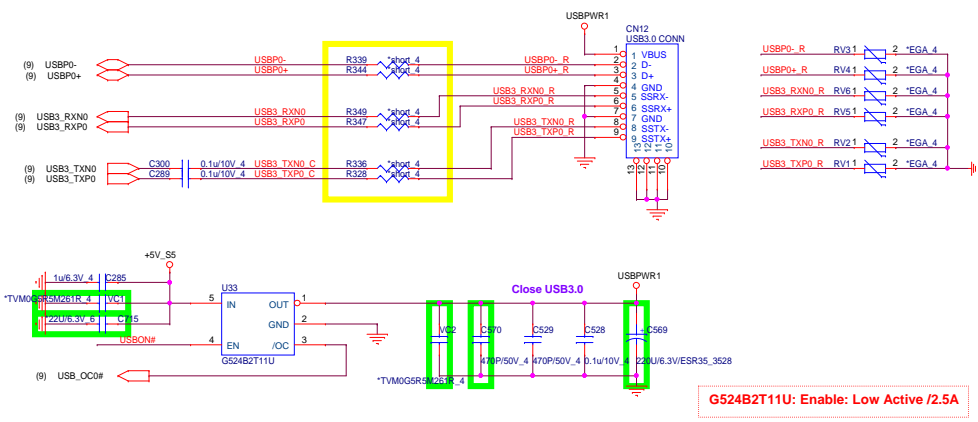
Layout: All termination
signal should have 30
mil trace

RJ45 Connector

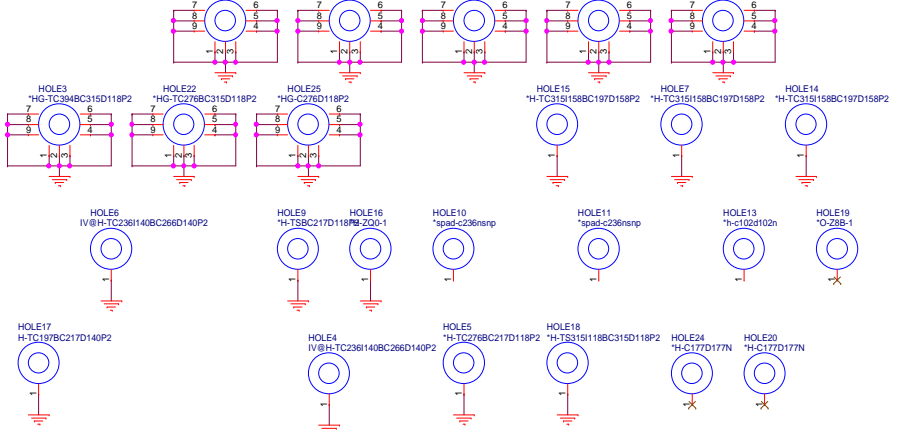


1A-7 2013/10/22 CN5006 pin9/10
add R5332/R5333 for RSD protect.

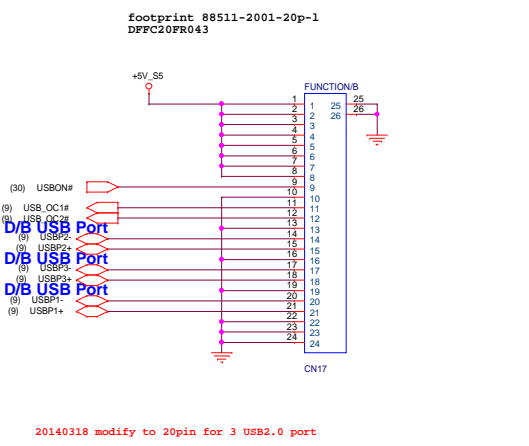
USB 3.0 Connector



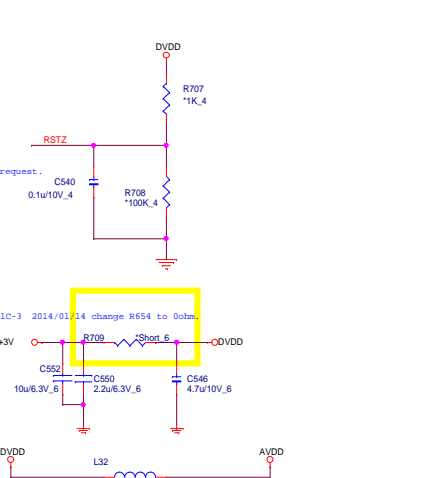
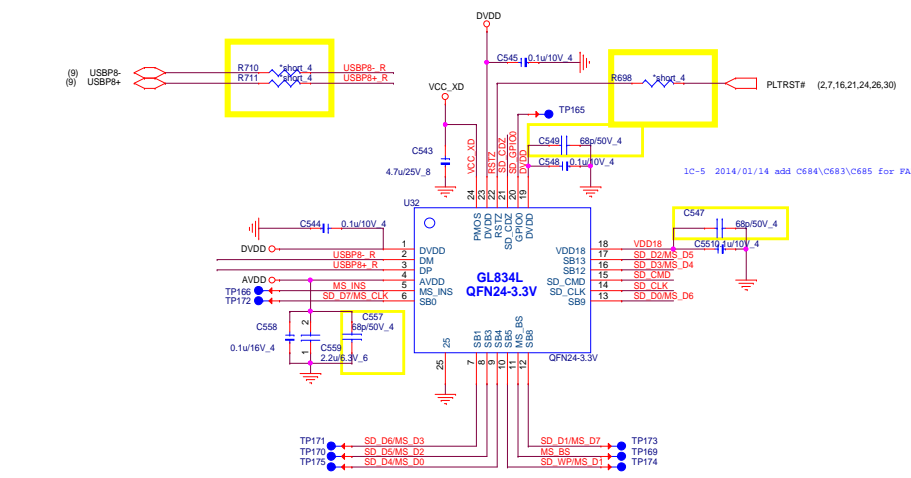
HOLE(OTH)



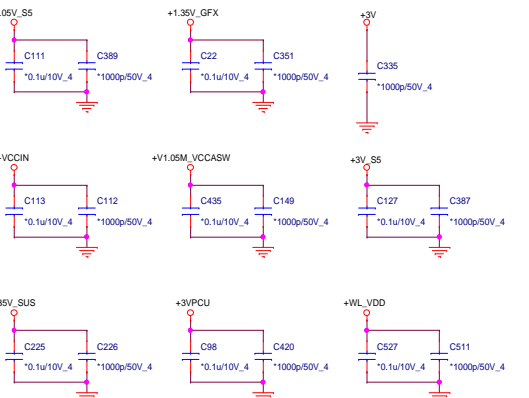
USB IO D/B



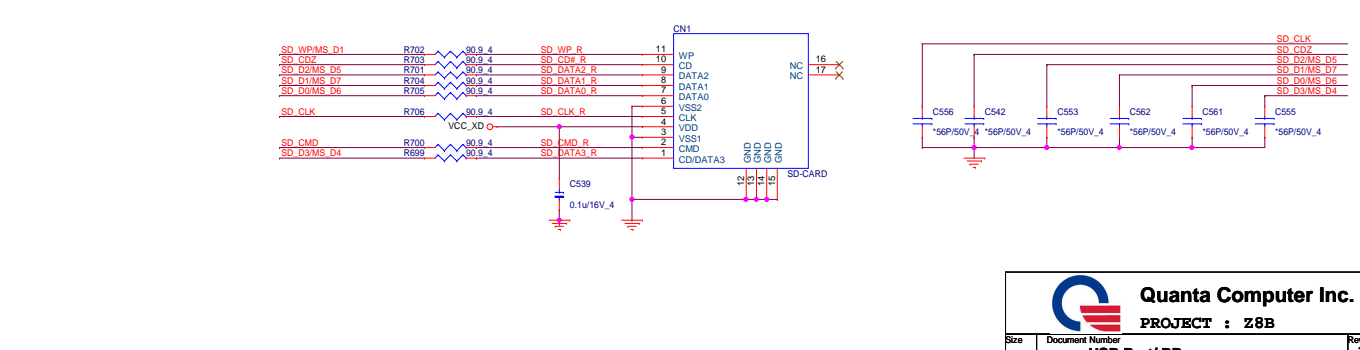
Card Reader and Connector

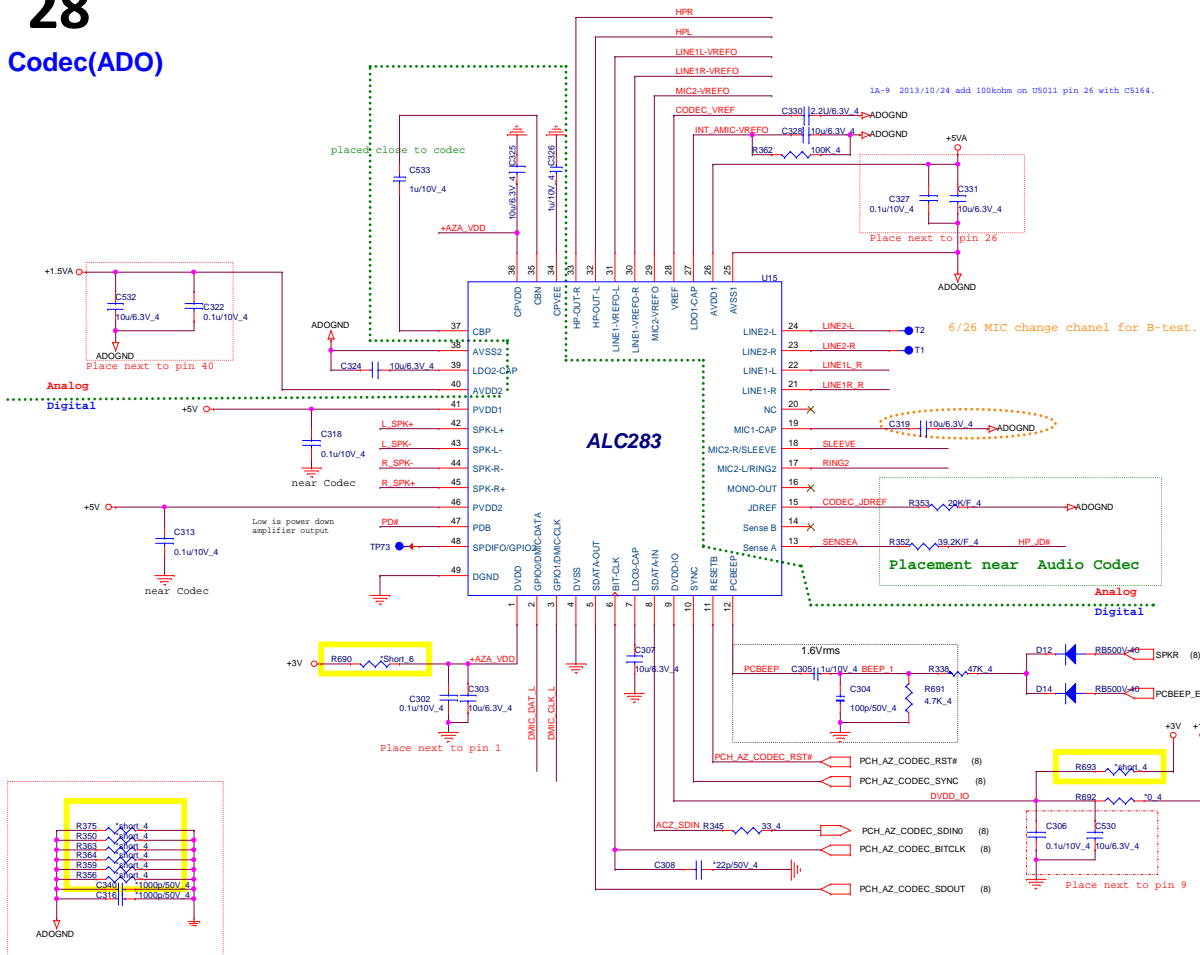


EMI

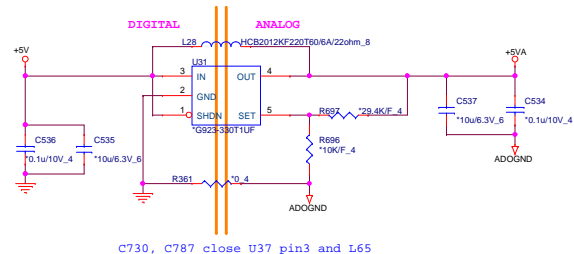


SD/MMC CARD READER (CRD)



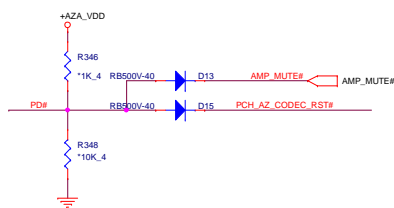


Codec PWR 5V(ADO)

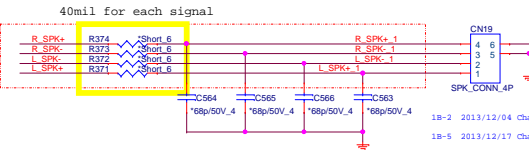


C730, C787 close U37 pin3 and L65

Mute(ADO)



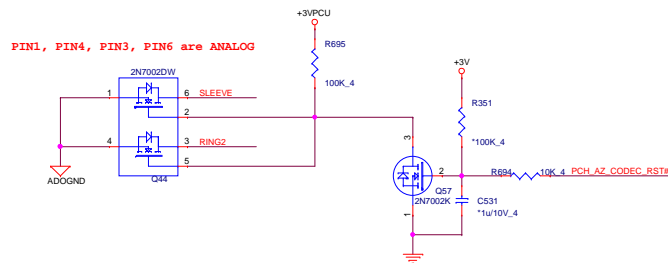
Internal Speaker



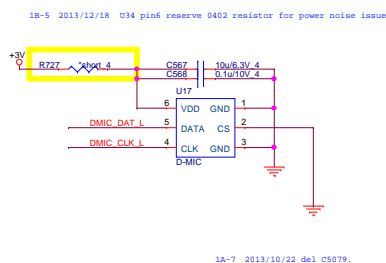
1B-2 2013/12/04 Change PW and footprint.

1B-5 2013/12/17 Change Q14 pin define

Grounding circuit(ADO)

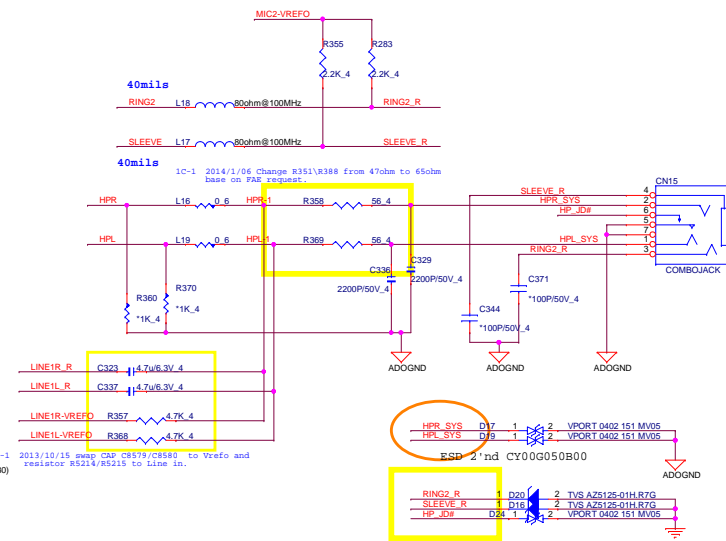


D-Mic



1A-7 2013/10/22 del C5079

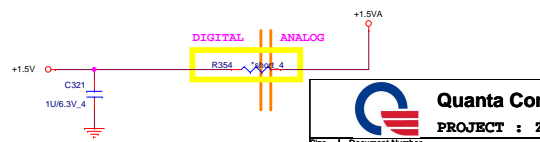
Universal Audio Jack



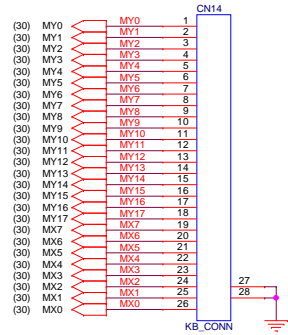
LA-1 2013/10/15 swap CAP C8579/C8580 to Vrefo and
resistor R5214/R5215 to Line in.

(30) resistor R5214/R5215 to Line in.

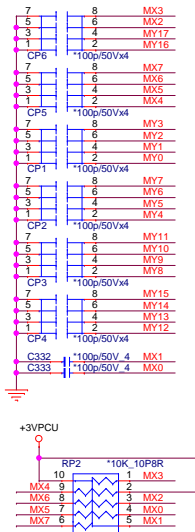
Codec PWR 3V/1.5V(ADO)



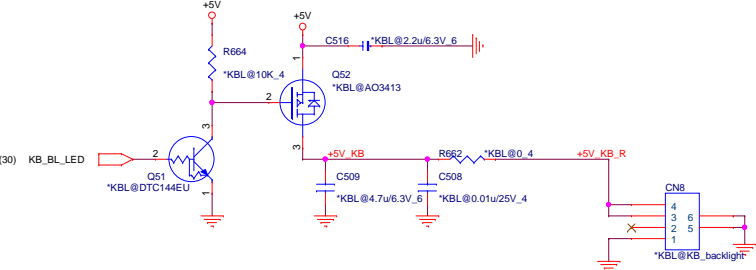
29 K/B (KBC)



1A-7 2013/10/22 change CN24 pin define based on spec.
1A-8 2013/10/22 change CN24 pin define based on spec based on Z8Q.

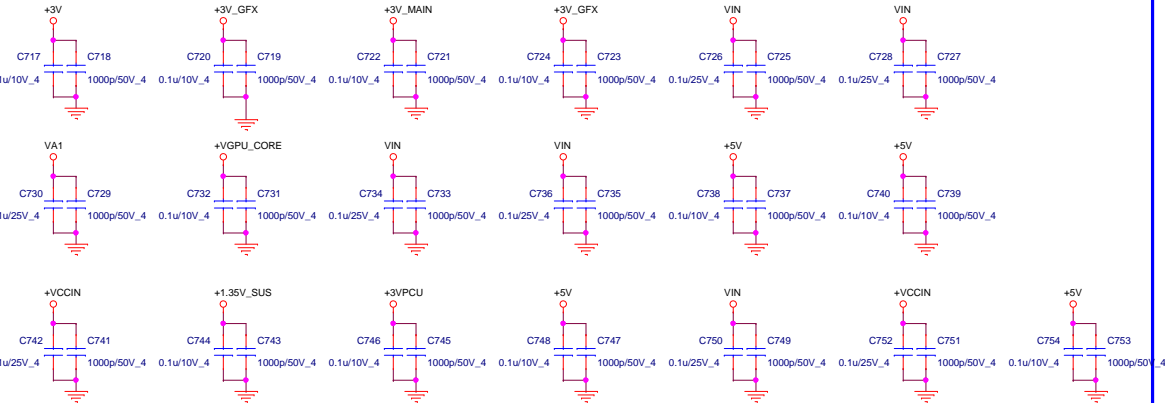


KB_BL LED (KBC)

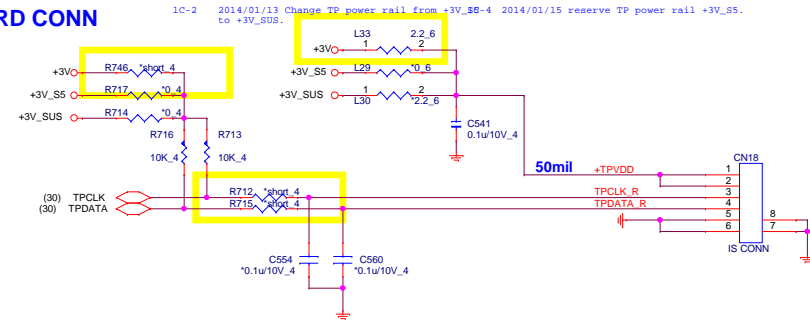


1A-7 2013/10/22 change CN25 pin define for spec.
1A-8 2013/10/23 change CN25 footprint.

EMI Cap



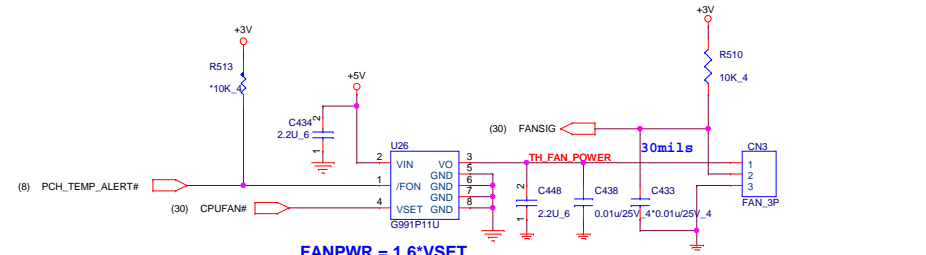
TOUCHPAD BOARD CONN



TPD->100KHz, TS=400KHz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u. TS=3x5inch
400KHz10-100u=2.4-0.4k.
100KHz 10-100u=9k-1k.

1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD identify.
2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,
1A-12 reserve PS2 PU to +3V.

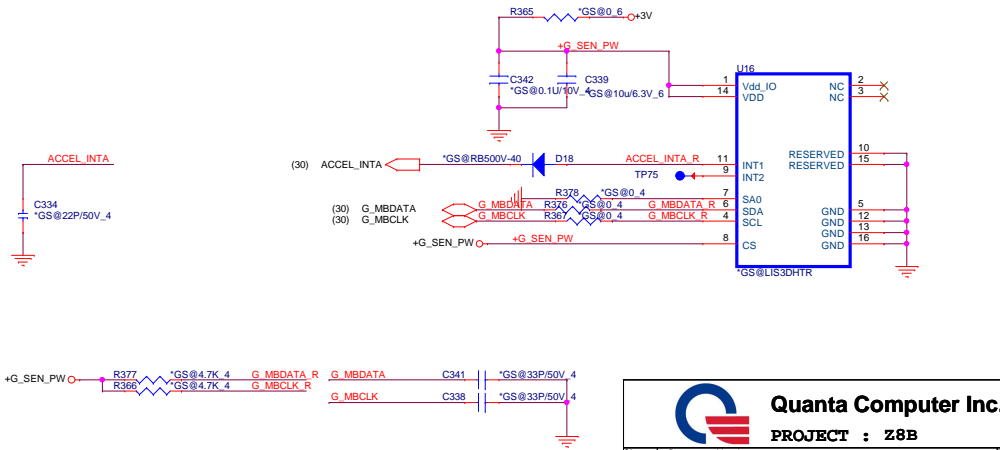
CPU FAN (THM)

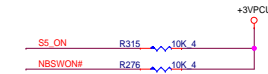
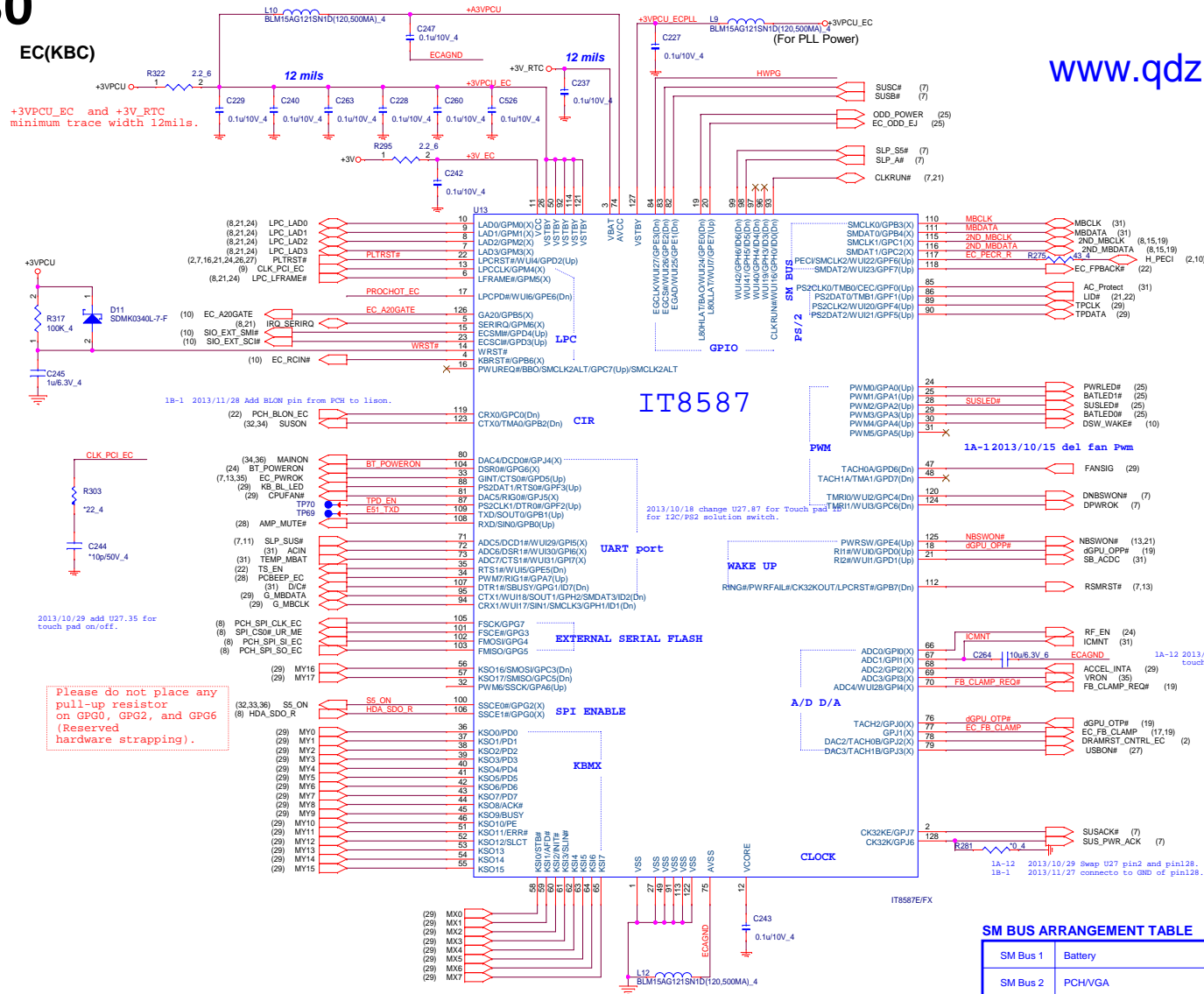


FANPWR = 1.6*VSET

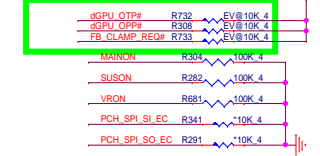
1A-12013/10/15 change pin define and add pwm IC U17.
1A-112013/10/15 change 30mils to 30mils and add G991P11U and PU U17 pin1.
1A-92013/10/24 Add alert on U17.1 for CPU thermal tempreture.

Accelerometer Sensor(reserve only)

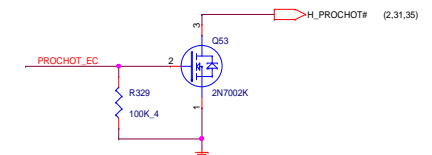
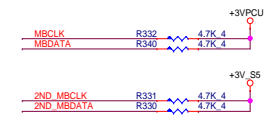




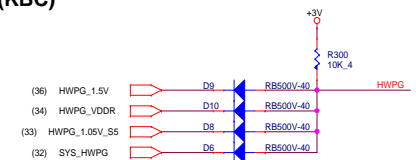
Add R732,R733



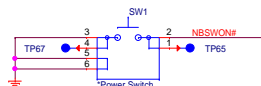
SM BUS PU(KBC)



HWPG(KBC)



For test only

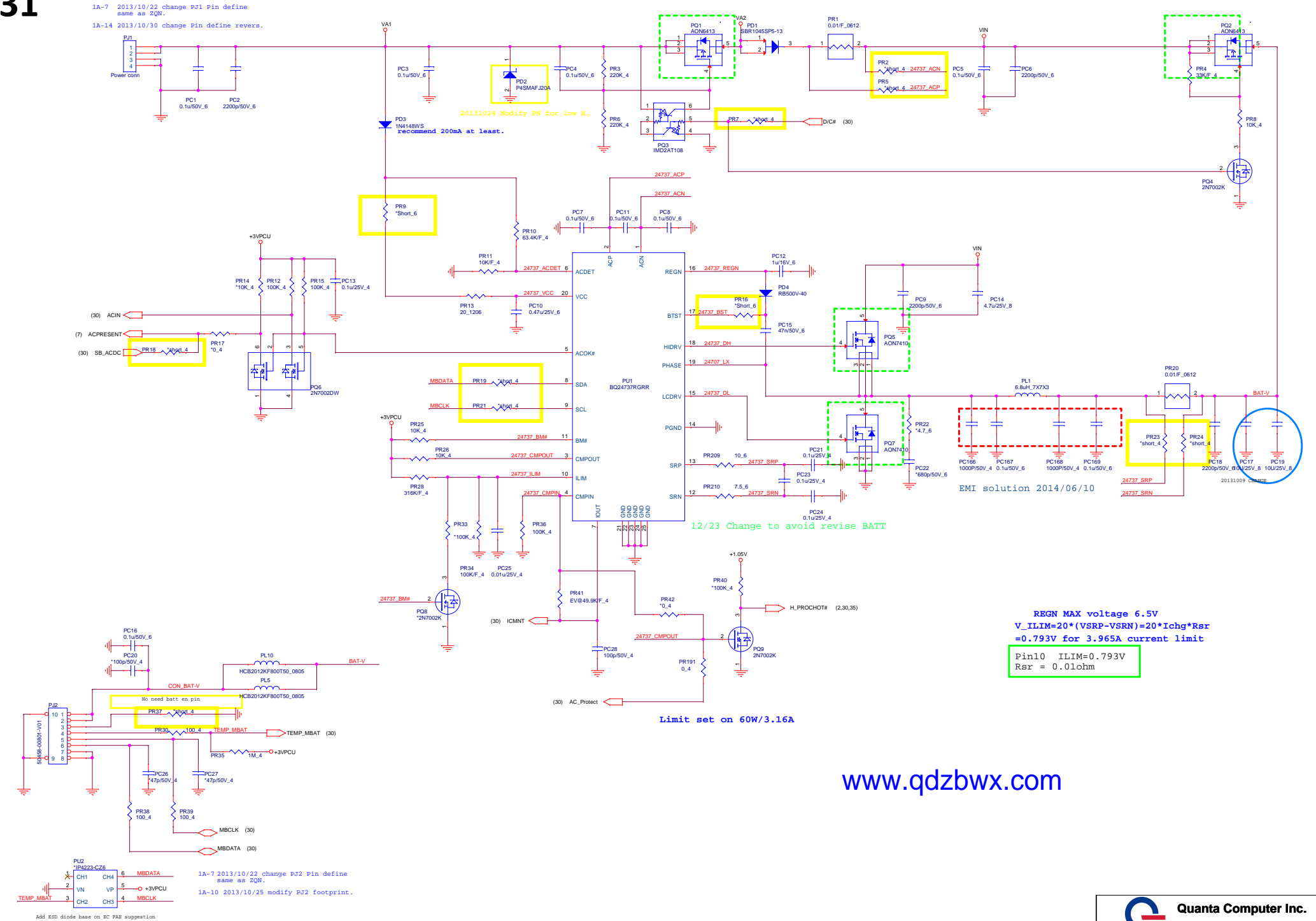


iRST

1A-4 2013/10/17 Del U22 becuse no support IOAC

SM BUS ARRANGEMENT TABLE

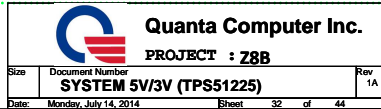
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	G-Snesor
SM Bus 4	

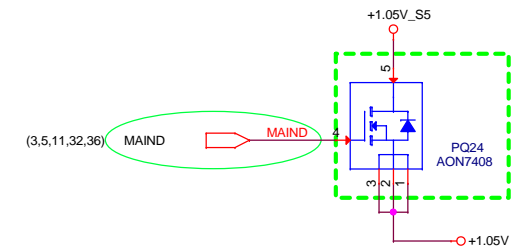
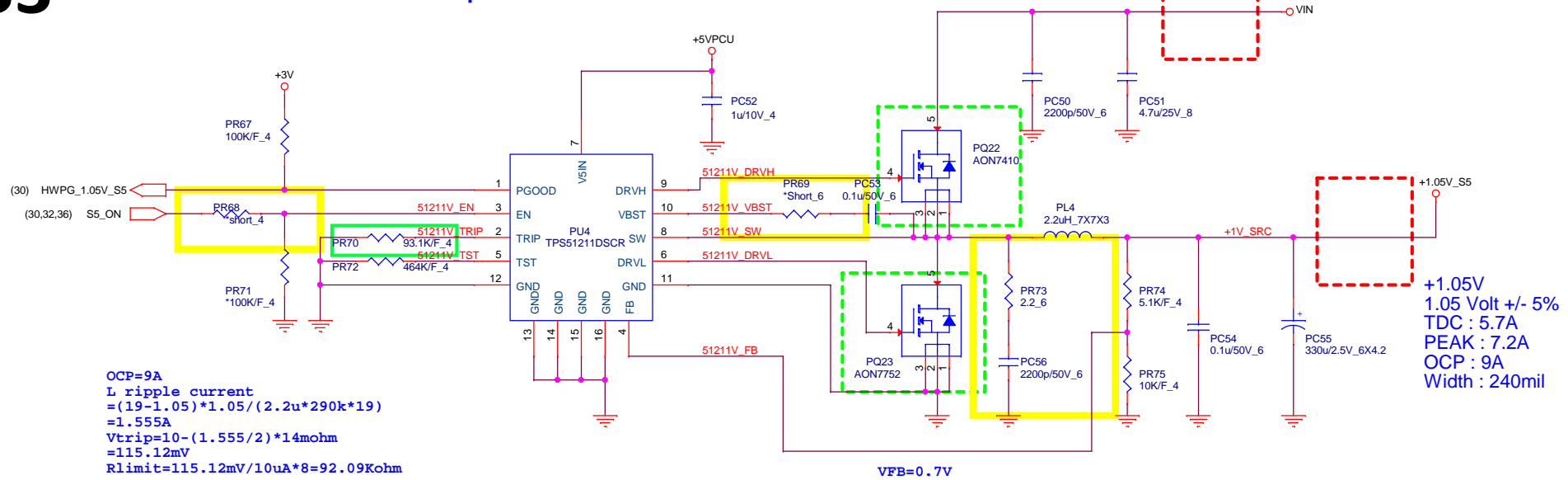


www.qdzbw.com

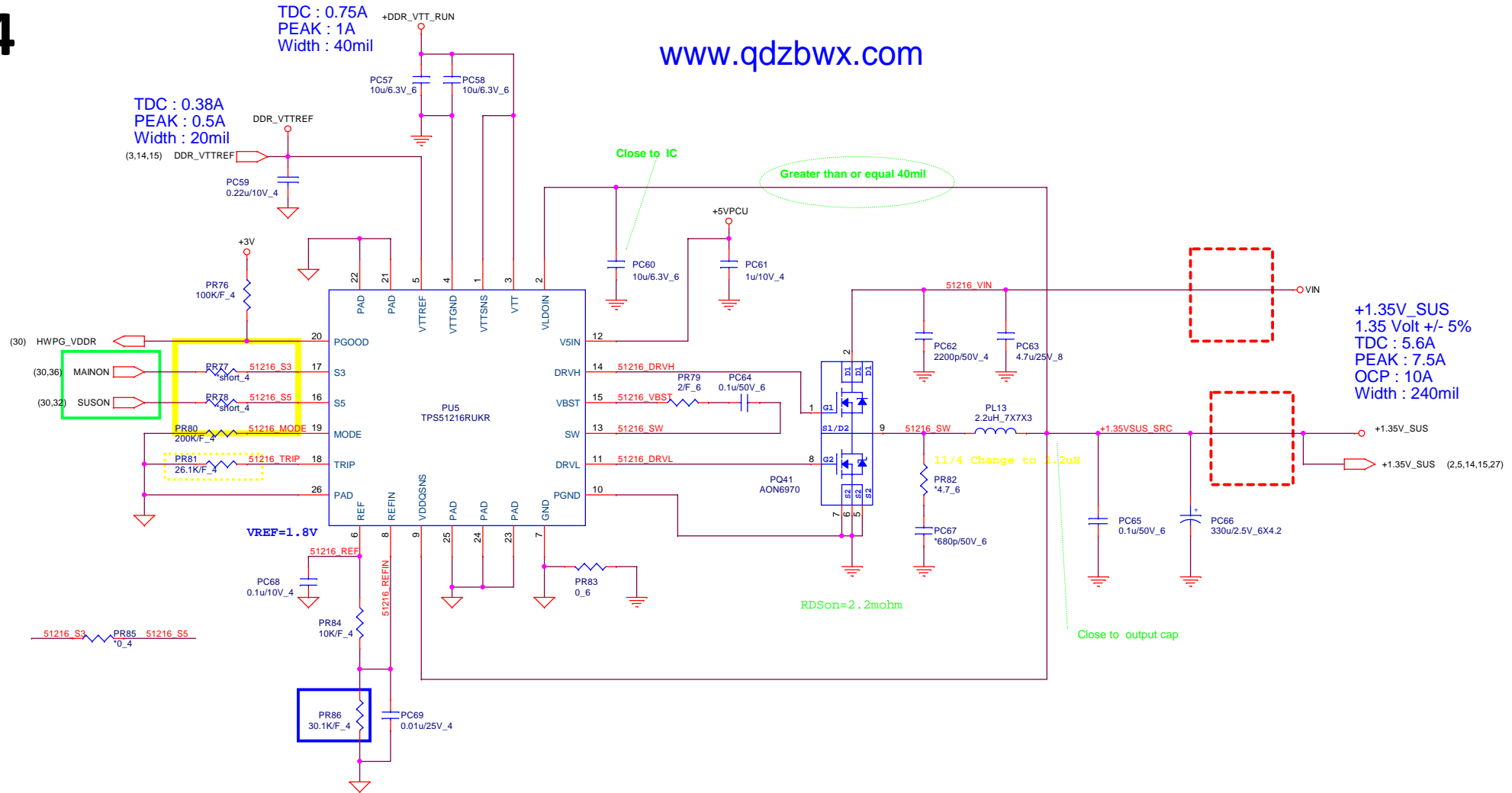


OCP:5A
L(ripple current)
 $= (9-3.3) \cdot 3.3 / (6.8 \mu \cdot 0.355 \text{M} \cdot 9)$
 $\sim 0.865 \text{A}$
 $I_{\text{ocp}} = 5 - (0.865 / 2) = 4.57 \text{A}$
 $V_{\text{th}} = 4.57 \text{A} \cdot 14 \text{m}\Omega + 1 \text{mV} = 64.94 \text{mV}$
 $R(\text{Ilim}) = (64.94 \text{mV} \cdot 8) / 10 \mu \text{A}$
 $\sim 51.95 \text{K}$





1B-2 2013/12/03 change PQ24 to DFN 3x3 size



OCP=10A
L ripple current
= (19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=10-(1.425/2)*2.2mohm
=20.432mV
Rlimit=20.432mV/10uA*8=16.35Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

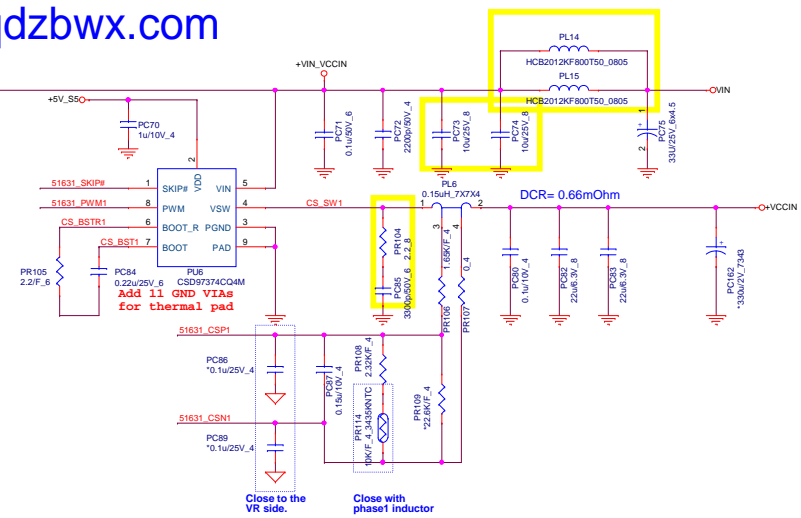
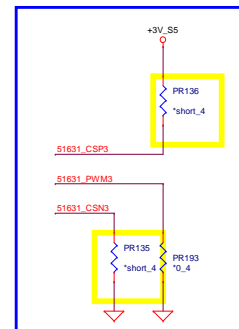
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

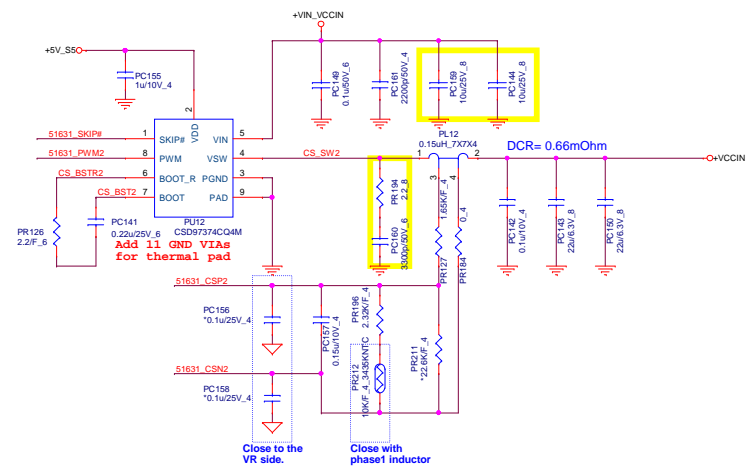


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DDR 1.35V(TPS51216)
Date: Monday, July 14, 2014 Sheet 34 of 44 Rev 1A

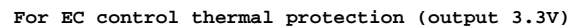


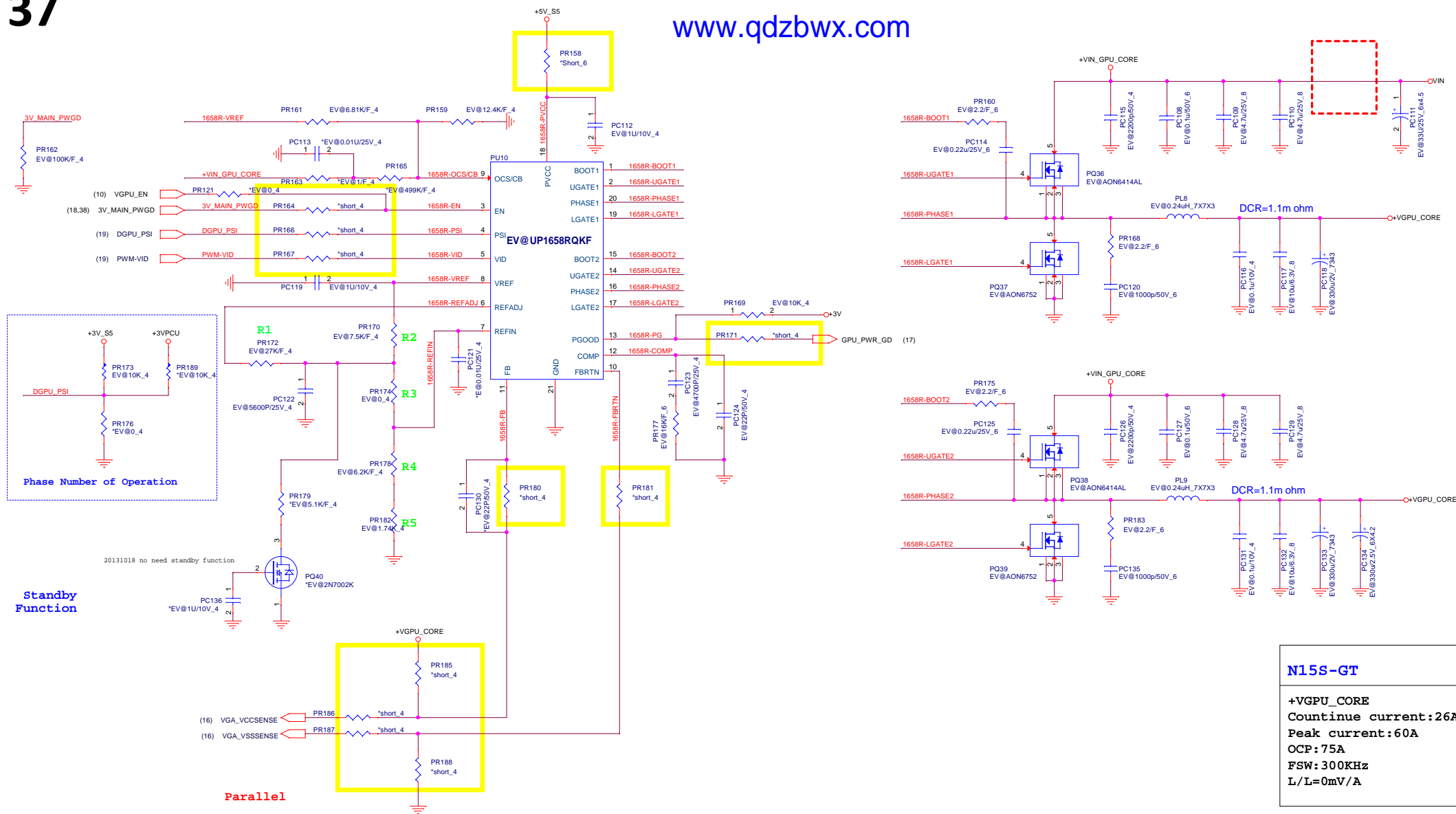
R_DC_LL : - 1.5mV/A
R_AC_LL : - 3.6mV/A





Need fine tune
for thermal protect point
Note placement position
TEMP=85C



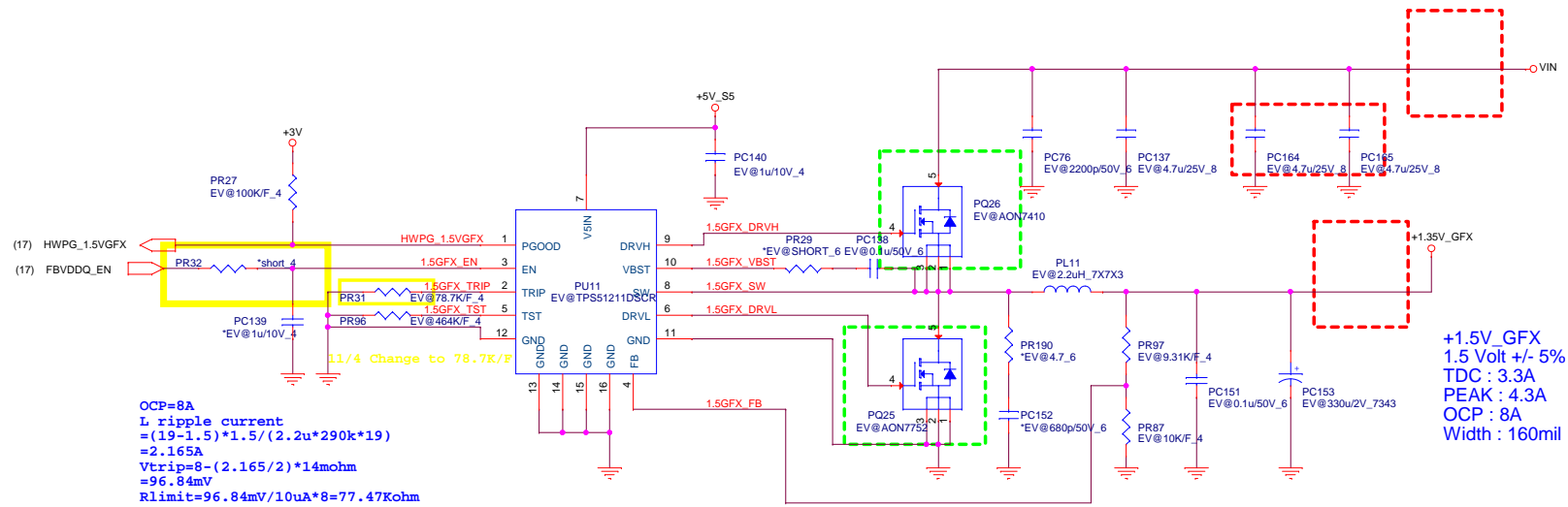
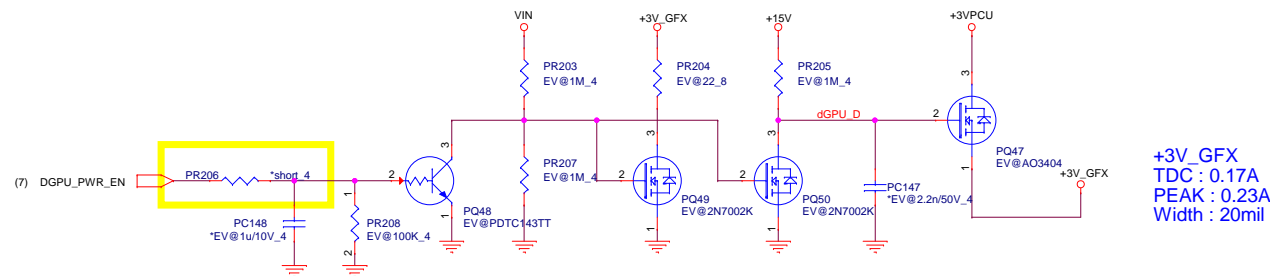
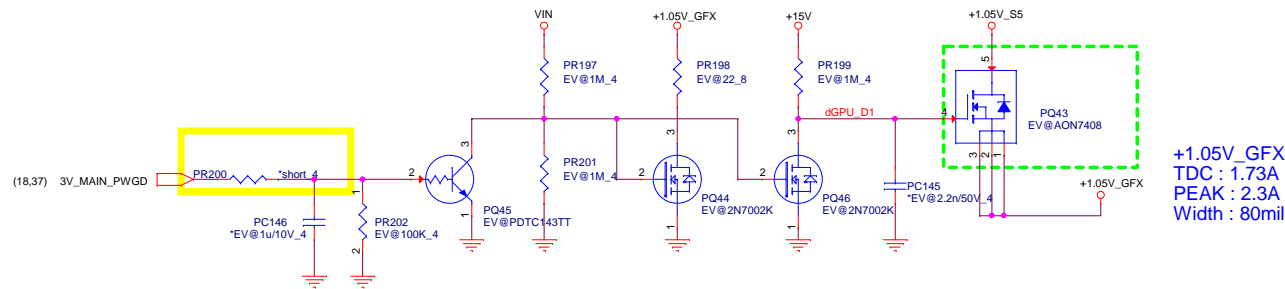


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Size Document Number Rev 1A
+VGPU_CORE(UP1642PQAG)

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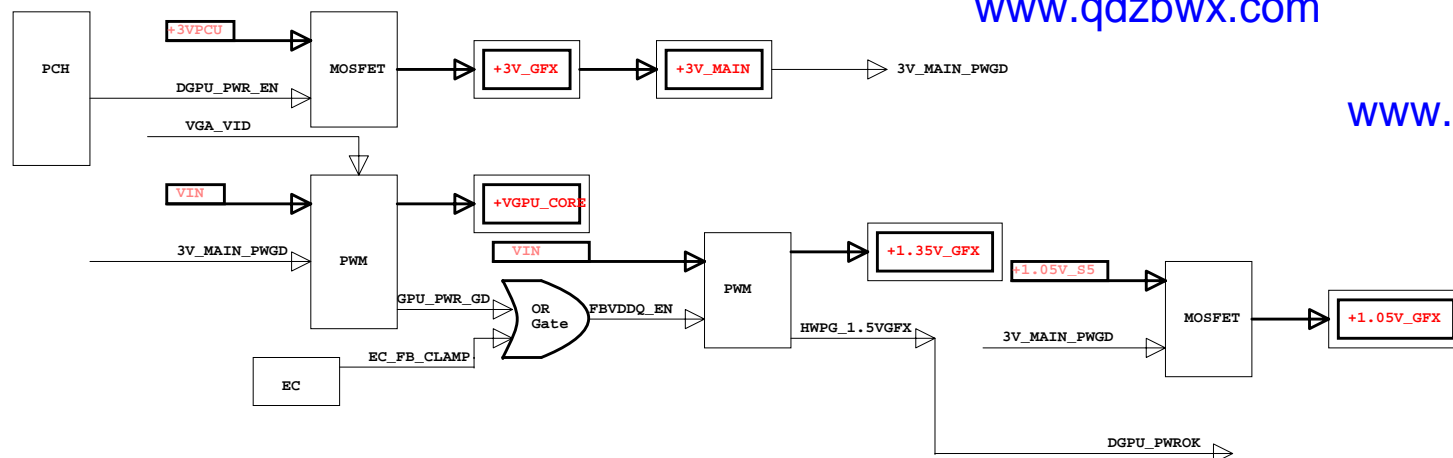
(16,17,18) +1.05V_GFX
(17,20,27) +1.35V_GFX
(16,17,18,19,30) +3V_GFX



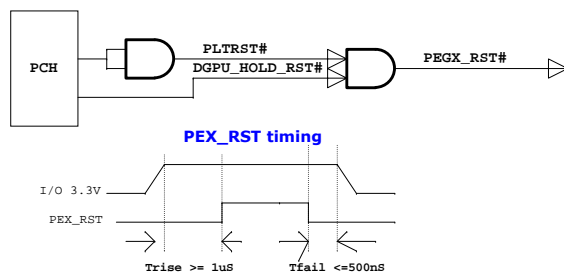
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Size	Document Number	Rev
	+1.35V_GFX/+1.05V_GFX/+3V_GFX	1A
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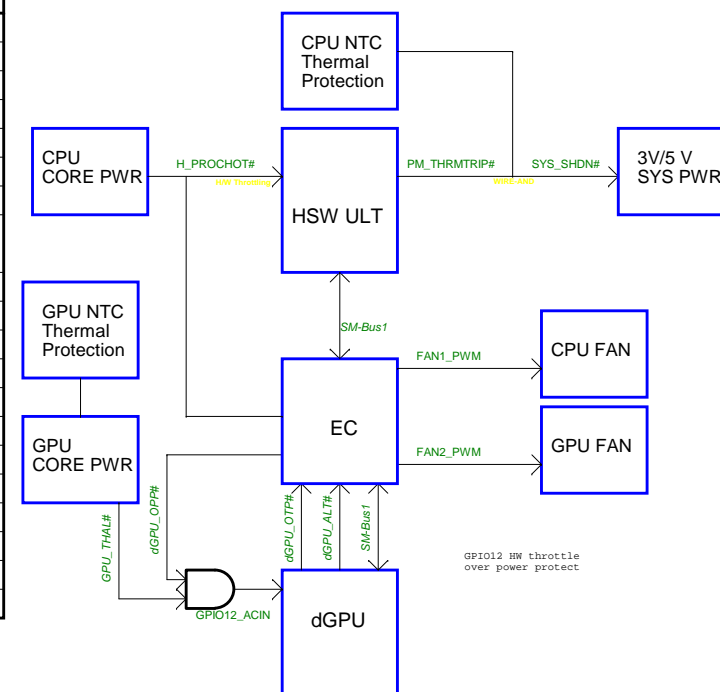
VGA Reset



Power States

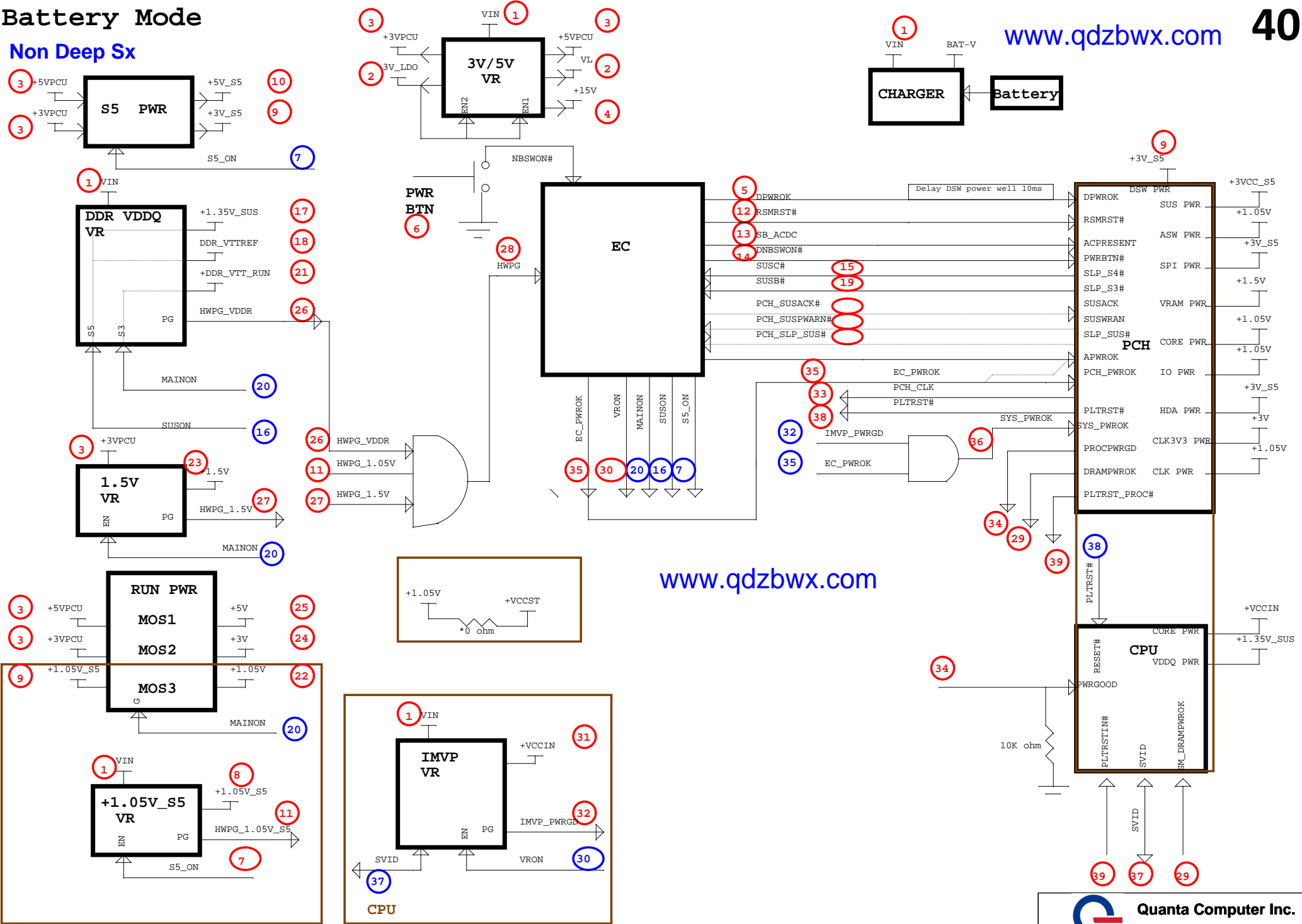
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V--+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V--+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+1.05V_S5	+1.05V	PCH CORE VCCST POWER& External GPU POWER	S5_ON	S0-S5
+5V	+5.0V	HDD/ODD/SPK/HDMI POWER/CRT	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	
LCDVCC	+3.3V	LCD POWER	EDP_VDD_EN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	
+3V_GFX	+3.3V	External GPU POWER	DGPU_PWR_EN	S0
+1.35V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	
+1.05V_GFX	+1.05V	External GPU POWER	3V_MAIN_PWDN	S0

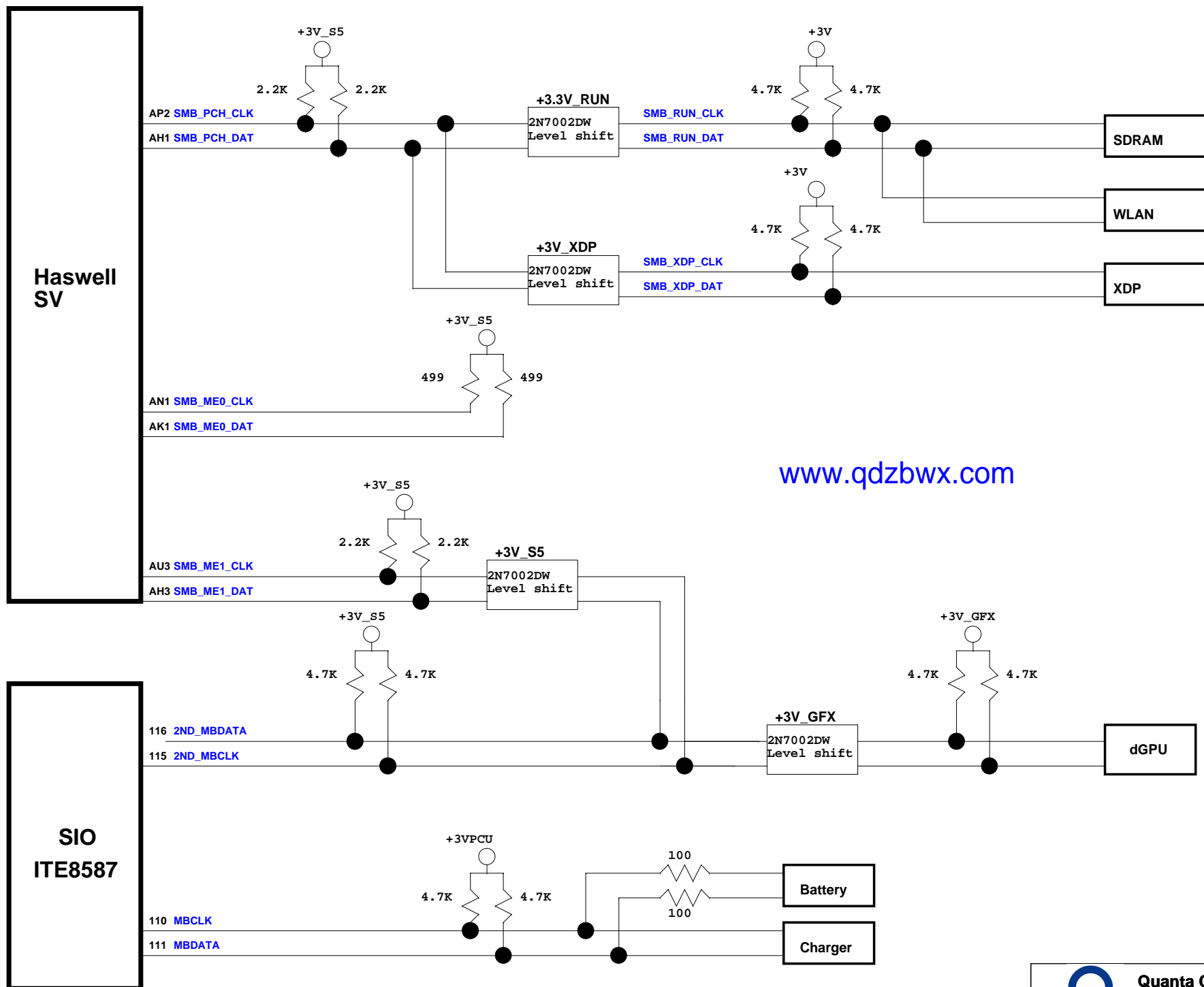
Thermal Follow Chart



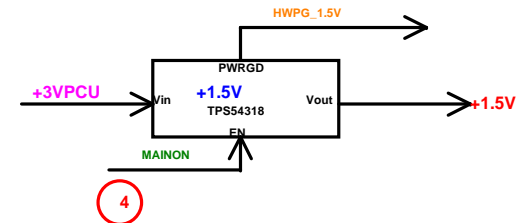
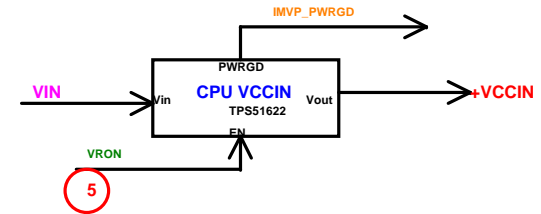
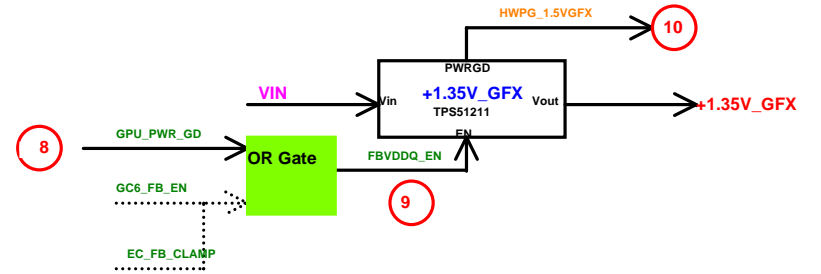
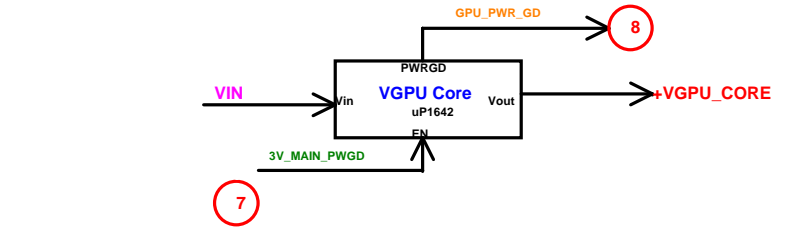
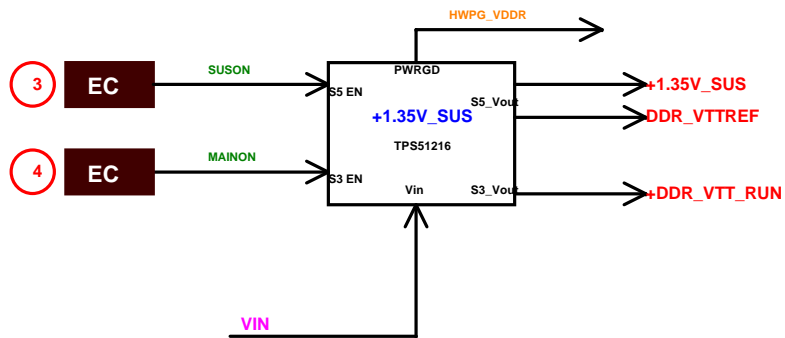
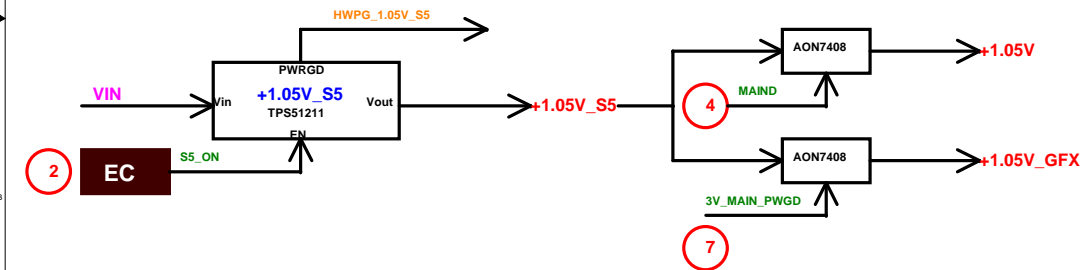
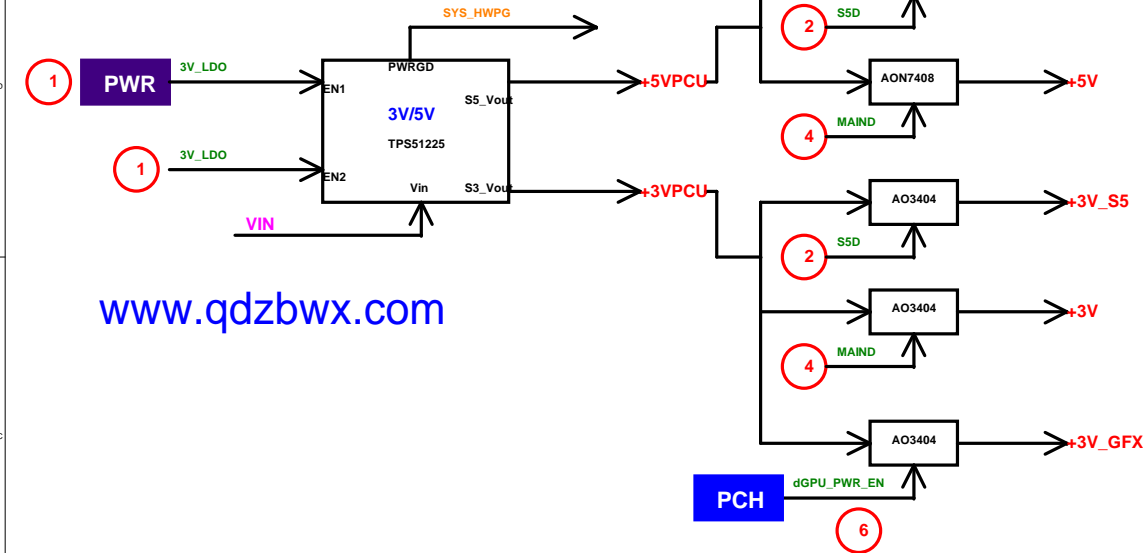
Battery Mode


Non Deep Sx





實線表default
虛線表reserve



Model	Version	CHANGE LIST			
EA41	1B-1	1 Stuff PE130 and PE134 (2014_05_30)→Add Voore sensing Resistor			
		2 Un stuff PC156 and PC158 (2014_05_30)→Remove Voore PWM cap to balance 2 phase driving current			
		3 Stuff R649 and R663 (2014_05_30)→Change for EEPROM QAUD MODE			
		4 Change R644 and R607 by CS21002B034 (2014_05_30)→Change for EEPROM QAUD MODE			
		5 Delete U3,U4,C319 and Add Q58,R729,R730,R731,D232(2014_06_09)→Change for CRT CCD level shift			
		6 Change Y3 from BGA25000737 to BGA250000H(2014_06_09)→Change for Parts EOD issue			
		7 Change R255 change 1.82K to 1.80K(2014_06_09)→Change for Parts EOD issue			
		8 Change C309,C310,C311,C312,C314,C315,C317,C320,C433,C438,C494,C496,C499,C508 from C0310030B11 to C0310040B17→Change for Parts EOD issue			
		9 Unstuff CP1,CP2,CP3,CP4,CP5,CP6,C332,C333 (2014_06_10)→Cost saving			
		10 Add J2 (2014_06_10)			
		11 Unstuff Q337 (2014_06_10)→Cost saving			
		12 Unstuff R308 (2014_06_10)→Solving Discrete issue			
		13 Add R732,R733 (2014_06_10)→Discrete issue			
		14 Delete U14,C283 Add U33,C569,C570 Add Location VC1,VC2,C715,C576,C569(2014_06_10)→Solving USB drop issue			
		15 Change R508,R509,R123,R256,R257,R192,R191,R455,R88,R59,R534,R524,R456,R311,R617,R625,R669,R208,R478,R211,R212,R348,R582,R583,R623,R218,R508,R501,R605,R163,R234 from Res 0 ohm 0402 to short pad→Cost saving			
		16 Change RP4,RP5,RP6 Add Location R74,R73,R76,R77,R78,R79→Cost Saving			
		17 Delete R522,R530→Cost saving			
		18 Change R577,R609,R641,R615 R165,R211 R610,R571,R611,R618,R215,R591,R602,R577,R607,R603,R613,R627,R508,R632,R638,R592,R488,R478,R616,R621,R569,R595,R619,R597,R228, R597,R553,R132,R564,R146,R141,R118,R132,R532,R276,RP7,R666,R485,R458, R720,R491,R487,R546,R536,R538,R507,R579,R557,R533,R558,R108,R502,R511,R577 from Res 0 ohm 0402 to short pad(2014_06_11)			
		19 Change R76,R55,R56,R108,R98, R99,R114,R87,R478,R127,R71,R81,R12,R143,R144,R525,R78,R95,R493,R312,R309,R335,R292,R286 from Res 0 ohm 0603 to short pad(2014_06_11)			
		20 Change R488,R54,R59,R64,R53,R626 from Res 0 ohm 0805 to short pad(2014_06_11)			
		21 Add PC166,PC167,PC168,PC169 for EMI solution			
		22 Delete JP11,JP12,JP13,JP4,JP10,JP7,JP14,JP5,JP3,JP9,JP2,JP1,JP8(2014_06_11)			
		23 Change PR192 from CS22742F800 RES CHIP 2.74K 1/16W + 1%(0402) to CS22492F822 RES CHIP 2.49K 1/16W + 1%(0402) (2014_06_11)→Power require			
		24 Change PR129 from CS41692F812 RES CHIP 160K 1/16W + 1%(0402)to CS41502F818 RES CHIP 150K 1/16W + 1%(0402) (2014_06_11)→Power require			
		25 Add PC164,PC165(2014_06_11)			
		26 Change R171 from CS43902B010 to CS43902B00(2014_06_11)			
		27 Change PC77 from C0433020B14 to C04472K0B00 (2014_06_11)			
		28 Change CN19 from DFHD04MB155 to DFHD04MB296 for SMT issue(2014_06_11)			
		29 Change CN16 from DFPC06F058 to DFPC06F127 by ME request(2014_06_11)			
		30 Change CN17 from DFPC20F043 to DFPC24F039 by ME request(2014_06_11)			
		31 Stuff C503(2014_06_12)			
		32 Unstuff R262 Stuff R259(2014_06_12)			
		33 Stuff R240(2014_06_12)			
		34 Stuff R271(2014_06_12)			
		35 Unstuff R247(2014_06_12)			
		36 Change U110 from AL09955K001 to AL099550000(2014_06_12)			
		37 Unstuff R603,R604(2014_06_12)			
		38 Delete R183 Add R323(2014_06_12)			
		39 Delete R062(2014_06_12)			
		40 Unstuff RY1,R32,R37,R39,R49,R50,R56, L13,L14,L15 Unstuff R339,R344,R349,R347,R336,R320(2014_06_12)			
		41 Hole-A,delete change from B7C363140BC234D140P2 to B7C2361140BC274D140P2(2014_06_12)			
		42 Unstuff R271 (2014_06_12)			
		43 Unstuff L11 and stuff R201, R299(2014_06_12)			
		44 Unstuff L31 and stuff R716, R713(2014_06_12)			
		45 Change R26,R286 from Res 0 ohm 0402 to short pad(2014_06_12)			
		46 Change R416,R417, R6 from Res 0 ohm 0603 to short pad(2014_06_12)			
		47 Change R17,R327 from Res 0 ohm 0805 to short pad(2014_06_12)			
		48 Change U32 from AL00834003 to AL00834004(20140613)→SD Card Issue			
		49 Change C417,C418 from C0810040B07(CAP CHIP 50V(-5%);C0C 0402) to C0810040B08(CAP CHIP 10P 50V(-5%);C0C 0402)(2014_06_13)→V3 EOD issue			
		50 Change L4 from C0800181016 to C03PE18100Q(20140613)→EOD issue			
		51 Change D22 from HCBAT54C204 to HCBAT54C232(20140613)→EOD issue			
		52 Change Q28,Q48,Q59 from BA001440207 to BA001440013(20140613)→EOD issue			
		53 Change Q13,Q14,Q22,Q21,Q25,Q27,Q29,Q33,Q34,Q38,Q46,Q54,Q55, from BANT70020001 to BANT70020002(20140613)→EOD issue			
		54 Change D4,D7 from BC88501V126 to BC88500V229(20140613)→EOD issue			
	1C-1	1 Add thermal-crimp schematic Add Location U2,Q39,Q40,C7 to R740,R741,R742(20140701)			
		2 Delete TPT for Assembly issue(20140701)			
		3 Add R743 for cost down(20140701)			
		4 Add TP17,TP178,TP179,TP180 for SMT issue(20140701)			
		5 Add TP181 for SMT issue(20140701)			
		6 Add C715,C716,C718,C719,C721,C722,C723,C724,C725,C726,C727,C728,C729,C730,C731,C732,C733,C734,C735,C736,C737,C738,C739,C740,C741,C742,C743,C744,C745,C746,C747,C748,C749,C750,C751,C752,C753,C754 for EMI filter(20140701)			
		7 Add PR41 CS44992F010 RES CHIP 49.9K 1/16W + 1%(0402) (20140704)			
		8 Add PR3a CS41002B020 RES CHIP 100K 1/16W 5%(0402) (20140704)			
		9 Add PR2a CS41002B020 RES CHIP 10K 1/16W 5%(0402) (20140704)			
		10 Add PR191 C080002B038 RESISTOR CHIP 0 1/16W + 5%(0402) (20140704)			
		11 Add PQ1 BANT70020002 TRANSISTOR MOS 2N7002Q(40V,300MA)SOT-23 (20140704)			
		12 PC2,PC3,C7,PC111 change from C043304MB02 to C043304MB03 for material prepare issue			
		13 C12,PC32,PC31 change from C06221M9A02 to C06221M9A00 for material prepare issue			
		14 Change R499,R202,R44,R412,R423,R279,R276,R656,R28,R31,R602,R606,R607,R665,R667,R668,R669,R670,R97,R195,R118,R691,R375,R358,R363,R364,R359,R356,R727,R354 from Res 0 ohm 0402 to short pad			
		15 Change R116, R562,R799,R690,R717,R372,R373,R374 from Res 0 ohm 0603 to short pad			
		16 Change R75,R101,R512,R142,R61,R477,R605 from Res 0 ohm 0805 to short pad			
		17 Delete PR2 Add R744,R745			
		18 Delete L21,L20			
		19 Change R379,R380,R381,R382 from RES 0 ohm 0402 to short pad(2014_07_09)			
		20 Delete L11 Change R299,R301 from RES 0 ohm 0402 to short pad(2014_07_09)			
		21 Delete L11 Change R299,R301 from RES 0 ohm 0402 to short pad(2014_07_09)			
		22 Delete L13,L14,L15 Change R339,R344,R345,R347,R336,R328 from RES 0 ohm 0402 to short pad(2014_07_09)			
		23 Delete L31 Change R718,R711 from RES 0 ohm 0402 to short pad(2014_07_09)			
		24 Change R718,R726 from RES 220 0402 1% to RES CHIP 2K 1% R725,R723 from RES 220 0402 1% to RES CHIP 400 1% (2014_07_09)			
		25 Add PQ1 R362 1/16W 5%0402 PC36 CAP 220P(2014_07_09)			
		26 Stuff R742 and on-stuff L30 (2014_07_09)			
		27 Change Hole 9 footprint from H708217011892 to H788-1 (2014_07_11)			
		28 Change CN1 footprint from subord-pads4-dqgls-cm04b 11p to subord 5-01301001000-6 11p-sm(2014_07_11)			
		29 Change Net: SERVE_A_R002_8 connection from A0D00 to D0ND (2014_07_11)			
		30 Add Net: HP_20W connection to D0ND (2014_07_11)			
		31 Unstuff L30 and R754,L30 and R746 connect to 3V (2014_07_12)			
		32 Add PR218 (2014_07_12)			
		33 Add Location PC170 (2014_07_14)			
		34 Change C53,C54 from CAP CHIP 10P 50V to CAP CHIP 8.2P 50V(2014_07_14)			
		35 Unstuff Q21,R382,R335,Q15,C22 and change R134 from 0805 0 ohm to short pad(2014_07_14)			
		36 Add PL14 and PL15 for reducing Vin noise(2014_07_14)			
		37 Change PR124 from RES CHIP 0 ohm 0805 to short pad (2014_07_14)			
		38 Change R481,R488,R712,R715,PR7,PR2,PR3,PR18,PR19,PR21,PR10,PR37,PR2,PR2A,PR45,PR46,PR8,PR15,PR16,PR17,PR23,PR25,PR135,PR136,PR139,PR154,PR156,PR157,PR185,PR186,PR187,PR188,PR189,PR181,PR17,PR200,PR204,PR32 from Res 0 ohm 0402 to short pad(2014_07_14)			
DOC NO.	PROJECT MODEL :	ZSB	APPROVED BY:	DATE:	
	PART NUMBER:		DRAWING BY:	REVISION:	
<div><div>Quanta Computer Inc.</div><div>PROJECT : ZSB</div><div>DRAWING : Change R664</div></div>					

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Model	Version	CHANGE LIST				
EA41	1C-1	<div><div>39 Change R481,R608,R712,R715,P167,P162,P165,P113,P121,P1191,P137,P123,P124,P145,P146,P168,P1115,P1116,P1117,P1122,P1131,P1123,P1125,P1135,P1136,R119,P1164,P1166,P1167,P1165,P1187,P1188,P1189,P1181,P1171,P1200,P1206,P162 from Res 0 ohm 0603 to short pad(2014_07_14)</div><div>40 Change R1,P193,P116,P163,P159,P156,P169,P177,P178,R118,P1131,P1158 from Res 0 ohm 0603 to short pad(2014_07_14)</div><div>41 Change P1504,P1514 from 0603,2.2ohm to 0603/2.2ohm(2014_07_14)</div><div>42 Change PC35,PC160 from 0603,1000pf to 0603/3300pf(2014_07_14)</div><div>43 Change PC73,PC74,PC146,PC11977cap from 4.7uf/25V/0805 to 10uf/25V/0805(2014_07_14)</div><div>44 Change R355,R35977from 64.5/15/0402 to 56/15/0402 (2014_07_14)</div><div>45 Delete PC81</div><div>46 Change TV5 Diode at D16 and D20(fromCY402M0402 to C512501200)(2014_07_15)</div></div>				
<div>www.qdzbwx.com</div>						
DOC NO.	PROJECT MODEL : PART NUMBER:	Z8B APPROVED BY: DRAWING BY:	 	DATE: REVISION:	 	<div><div>Quanta Computer Inc.</div><div>PROJECT : Z8B</div><div>Change list-1</div></div>